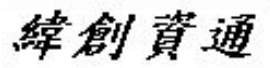


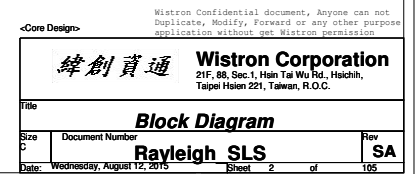
Rayleigh_SLS

Schematics Document

<Core Design>

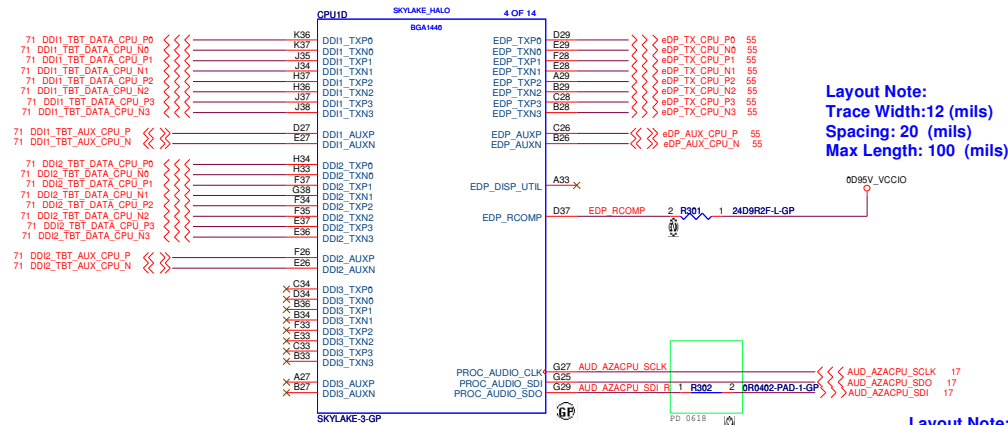
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
Size A	Document Number Rayleigh SLS		Rev SA
Date: Wednesday, August 12, 2015		Sheet 1	of 105

Project code :
PCB P/N :
Revision :

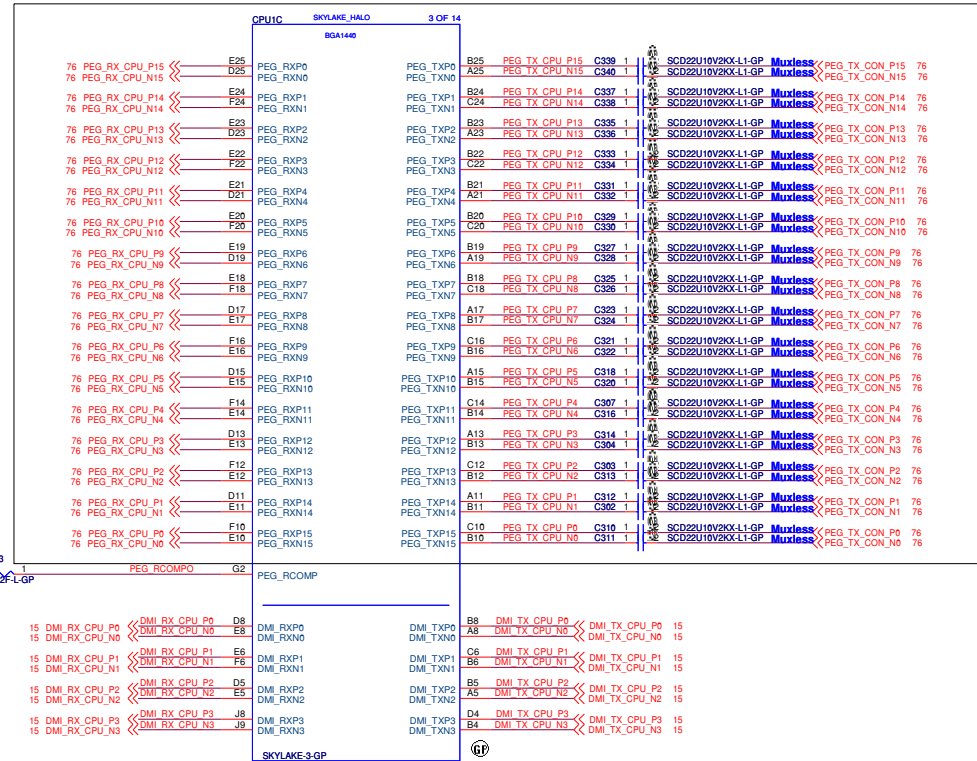


SSID = CPU

JJ 20150205 REVERSE PEG BUS



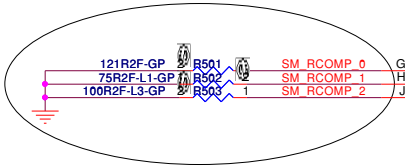
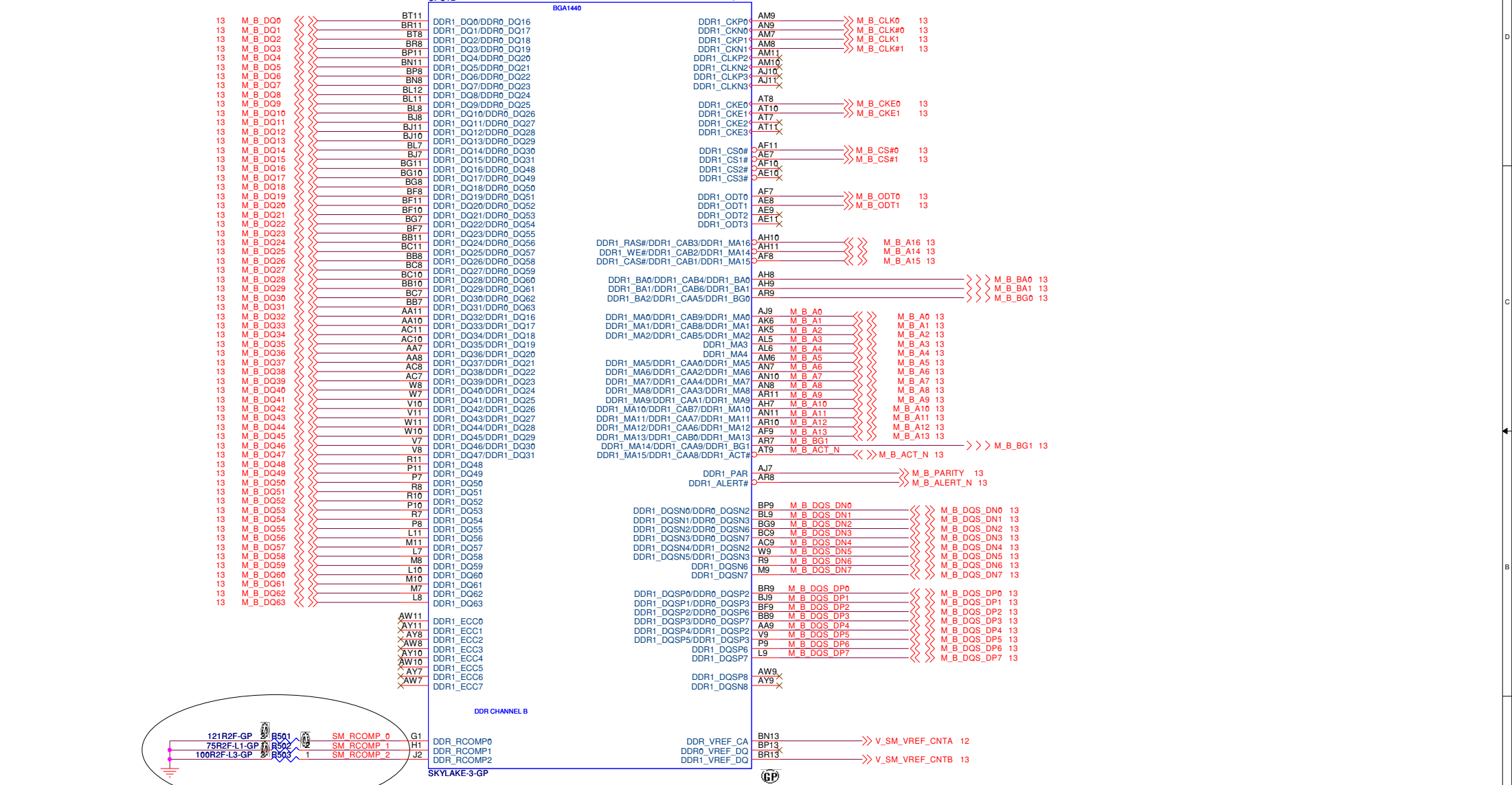
Layout Note:
Trace Width: 12 (mils)
Spacing: 15 (mils)
Max Length: 400 (mils)



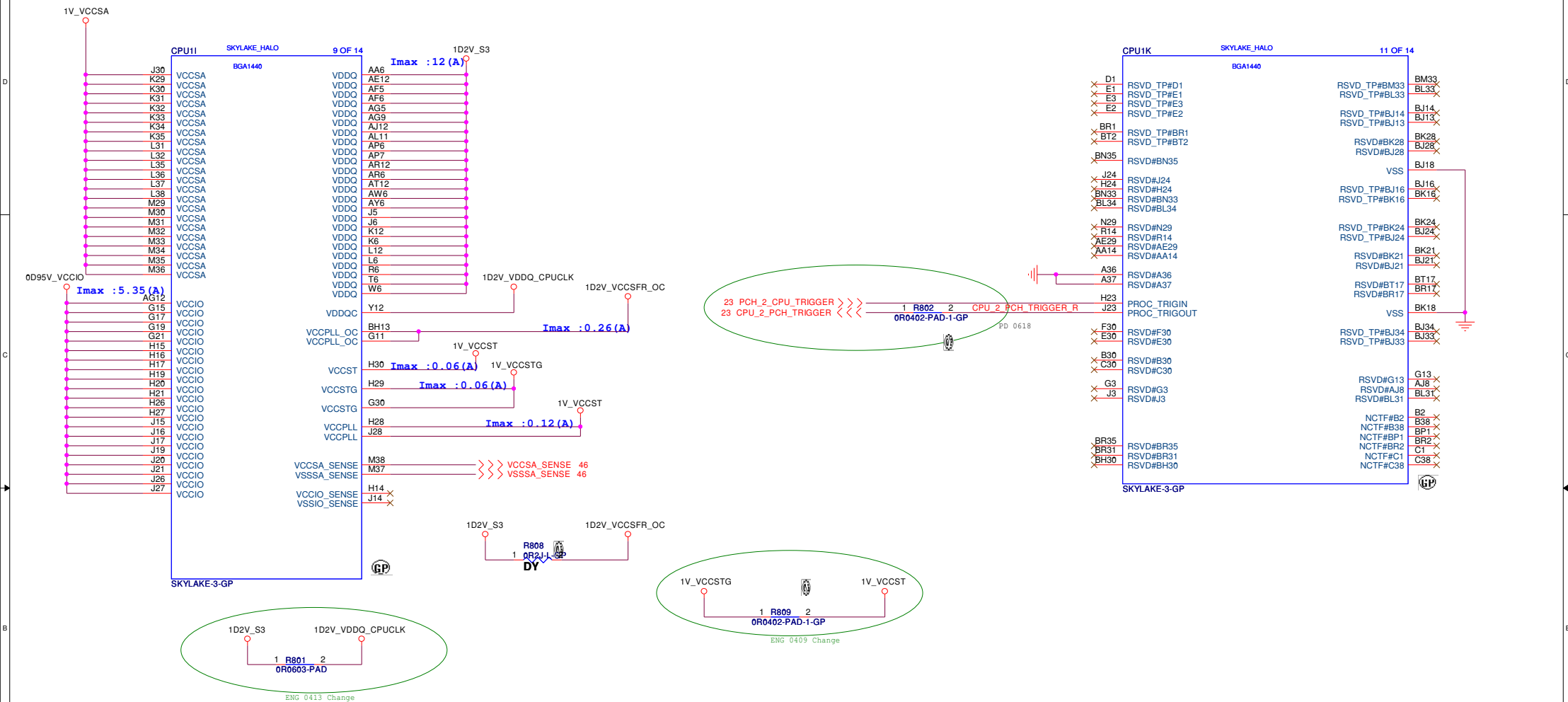
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Title			
CPU (PCIe/DMI/FDI)			
Size Custom			Rev SA
Document Number Rayleigh_SLS			
Date: Wednesday, August 12, 2015	Sheet 3	of 105	



SSID = CPU



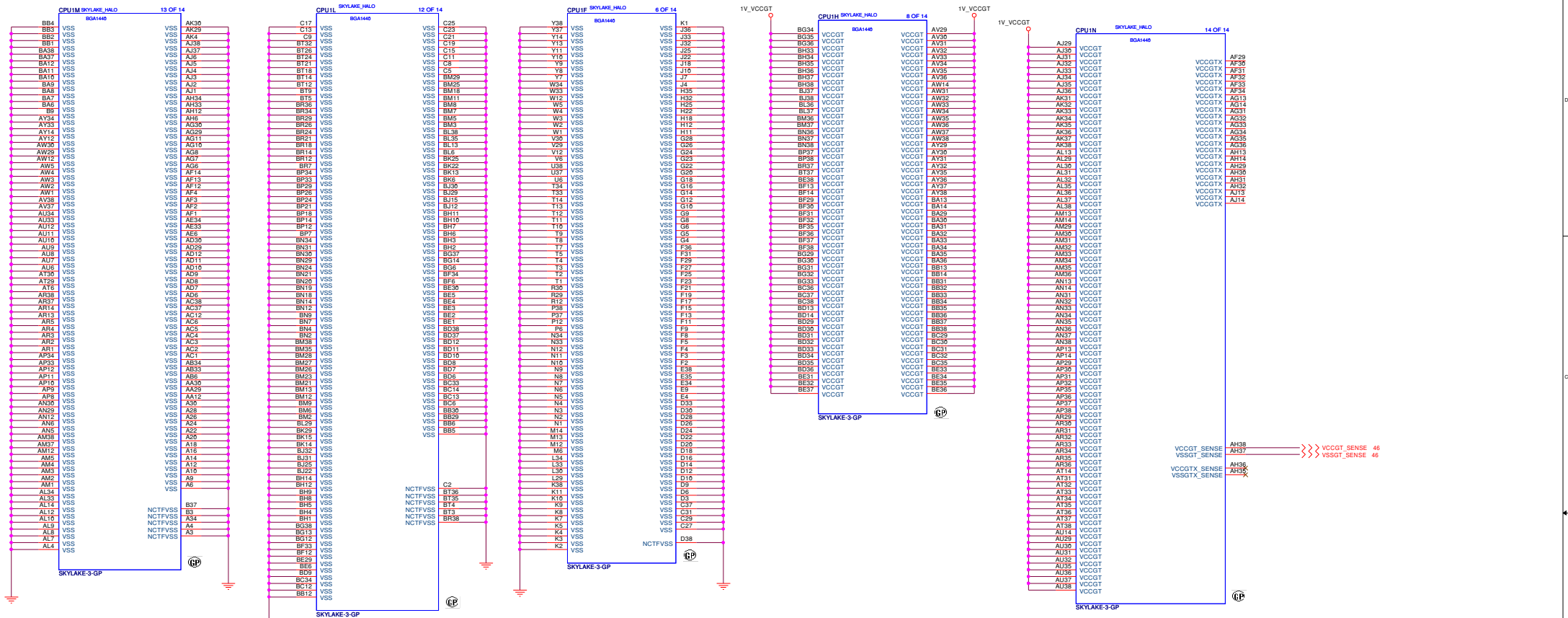
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Title			
CPU_POWER2(ASIC Power Bolck)			
Size A3	Document Number	Rayleigh_SLS	Rev SA
Date:	Wednesday, August 12, 2015	Sheet 8 of	105

SSID = CPU

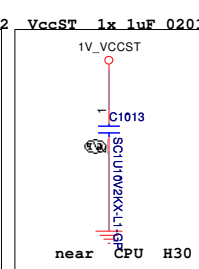
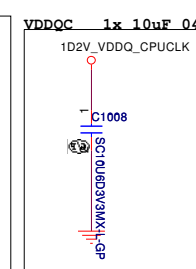
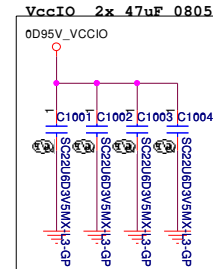
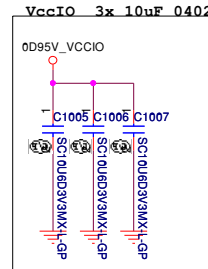
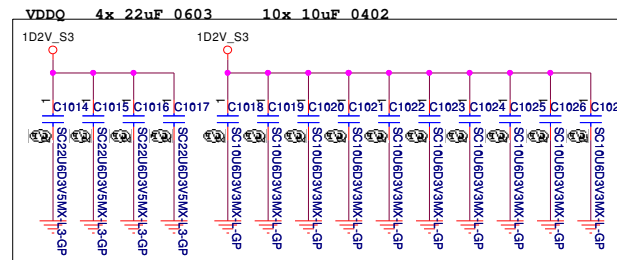
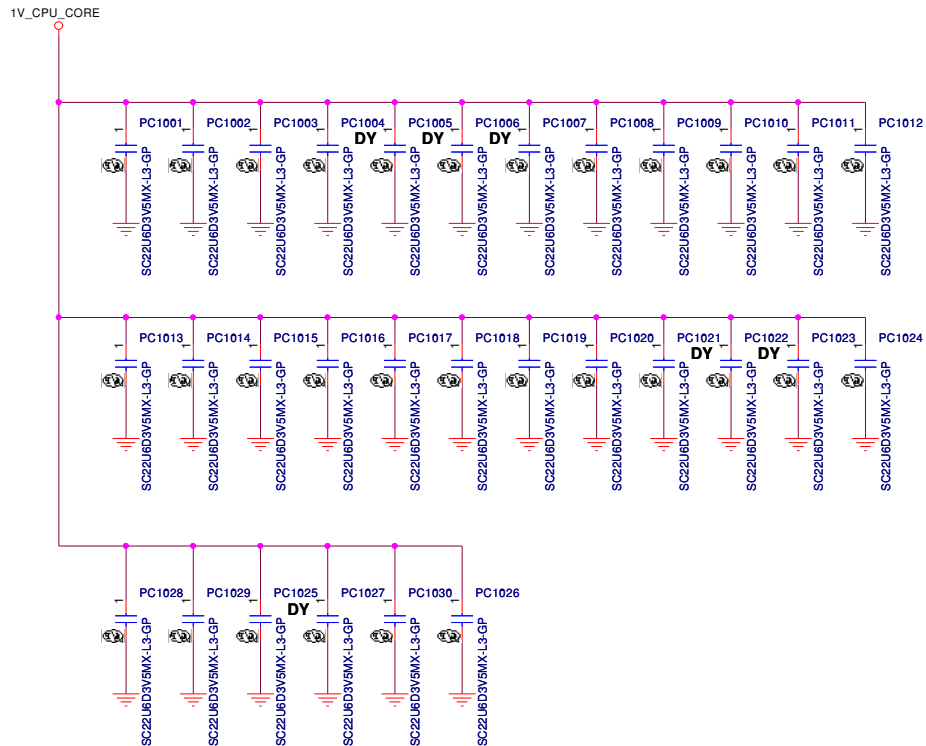


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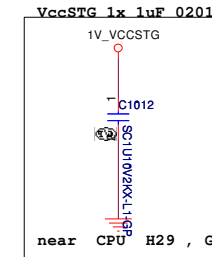
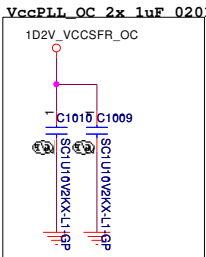
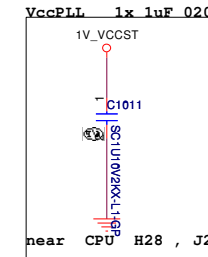
緯創資通

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File CPU_POWER3(ASIC Power Bolck)
Size A2 Document Number Rayleigh_SLS Rev SA
Date: Wednesday, August 12, 2015 Sheet 8 of 105



VR: +/-5% or +/-50mV
Place close to VR output



JJ 20150130

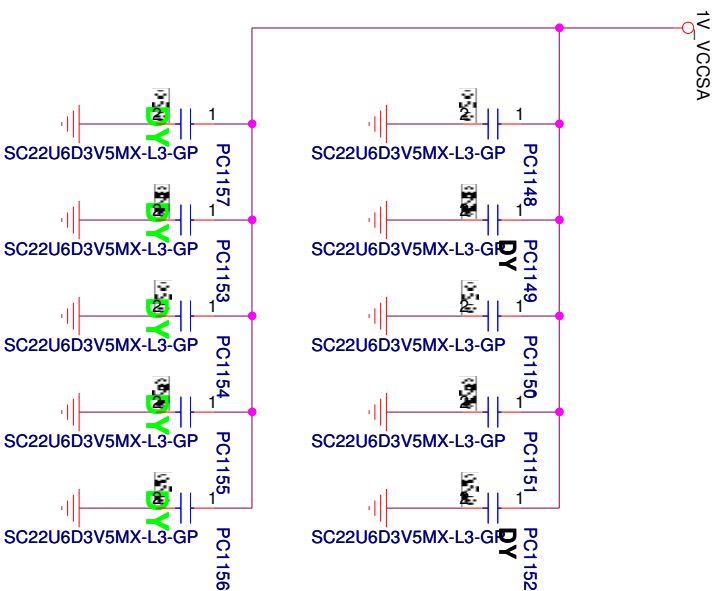
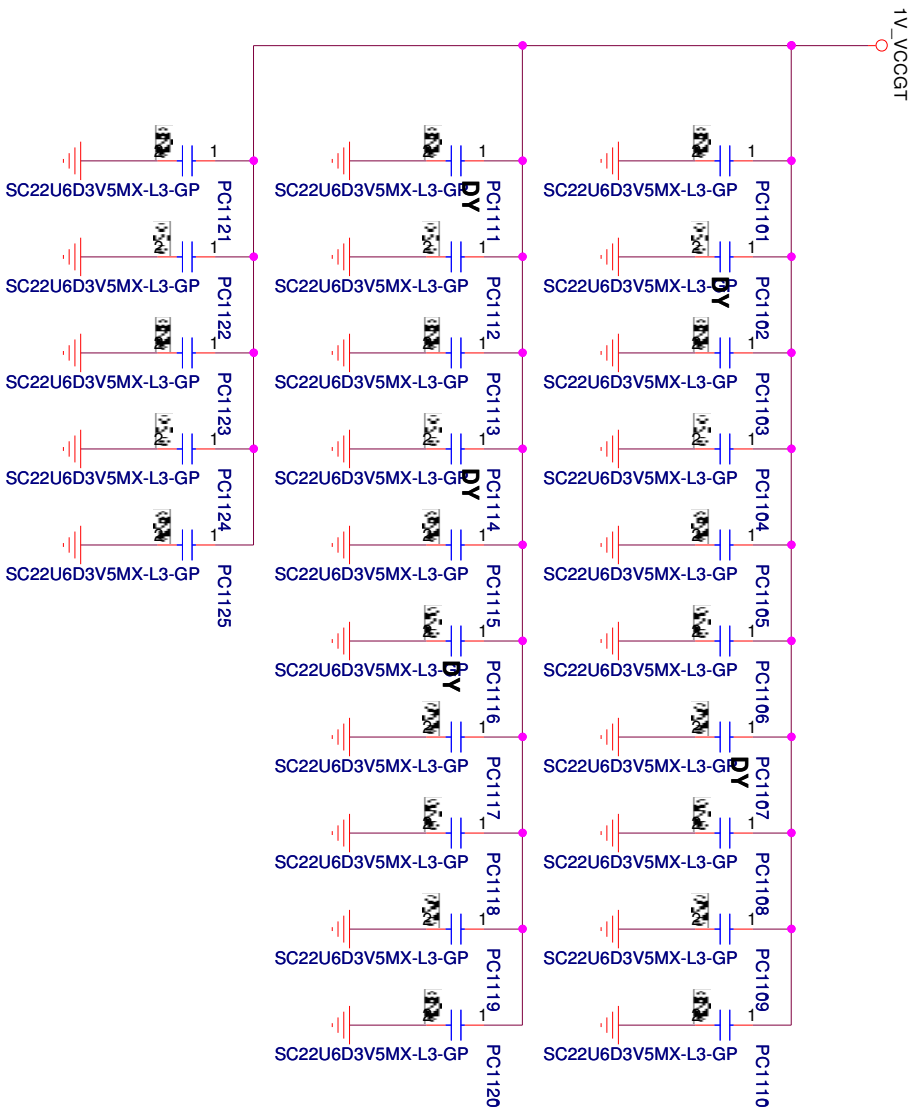
Decoupling Requirements for SKL H Processor (Sheet 2 of 2)

Domain	Board Edge cap	Backside cap	Notes
VCCGT	6x 47uF 0805	8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
VDDPDR	8x 22uF 0603	4x 10uF 0402	
		12x 1uF 0201	
VDDSA	1x 47uF 0805	1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
VDDQ		4x 22uF 0603	Share supply with DRAM
VDDQC		10x 10uF 0402	
VCCIO	2x 47uF 0805	1x 10uF 0402	VR: +/-5% or +/-50mV Place close to VR output
VCCST		3x 50uF 0402	
VCCST		1x 1uF 0201	Share supply with 1.0V PCH rail
VCCSTG		1x 1uF 0201	
VCCPLL		1x 1uF 0201	
VCCPLL_OC		2x 1uF 0201	Supply from 1.2V VDDQ
VCCORE		10x 10uF 0402	VR: +/-5% or +/-50mV
VCCPPDR		3x 10uF 0402	VR: +/-5% or +/-50mV

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Title	010 CPU (Power CAP1)		
Size A3	Document Number	Rayleigh_SLS	Rev SA
Date: Wednesday, August 12, 2015	Sheet 10	of	105



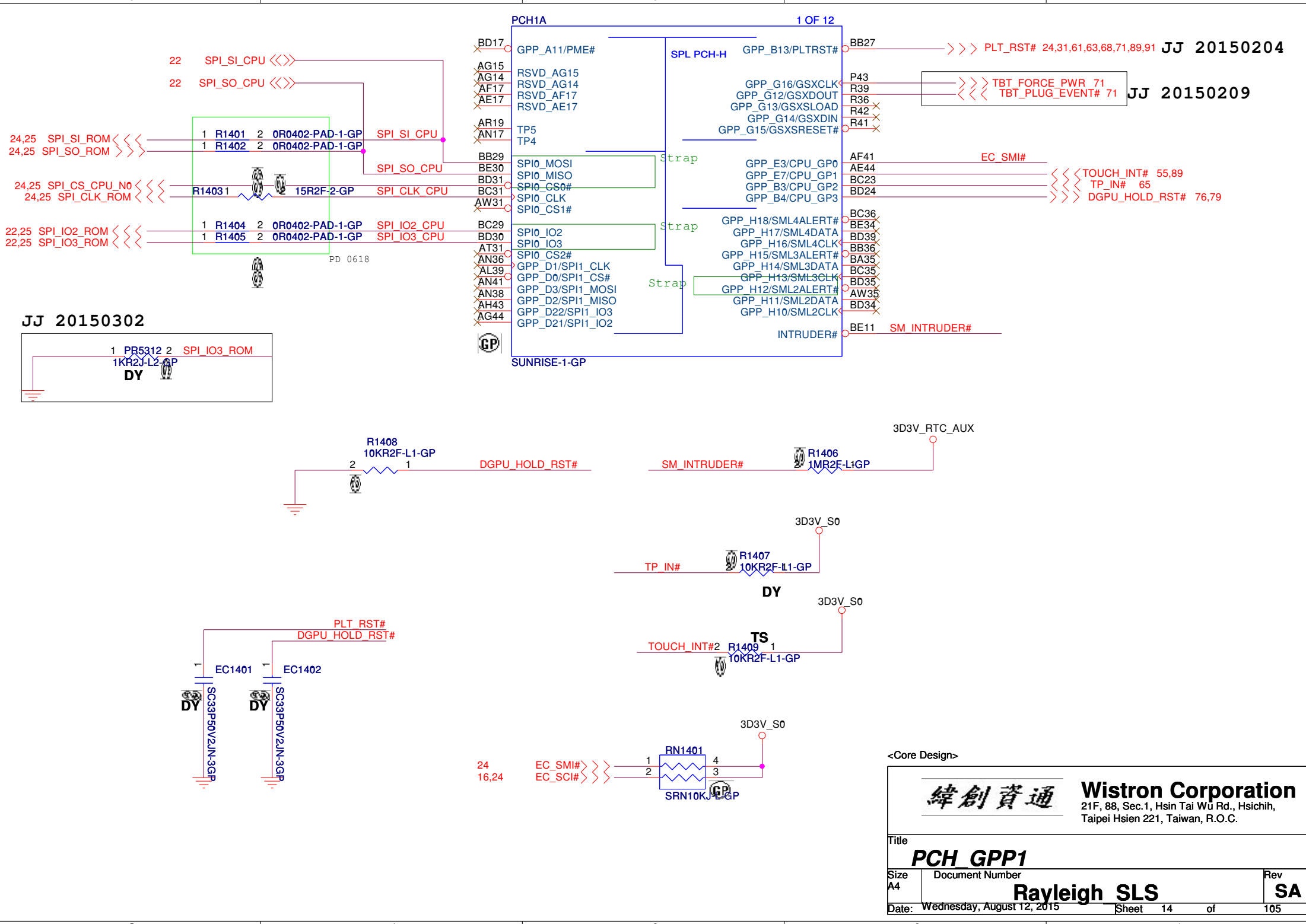
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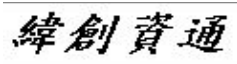
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CPU (Power CAP2)

Title		Rev	
Size	Document Number	SA	
A4	Rayleigh_SLS	105	
Date:	Wednesday, August 12, 2015	Sheet	11 of 105



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH GPP1			
Size A4	Document Number Rayleigh SLS		Rev SA
Date: Wednesday, August 12, 2015		Sheet 14	of 105

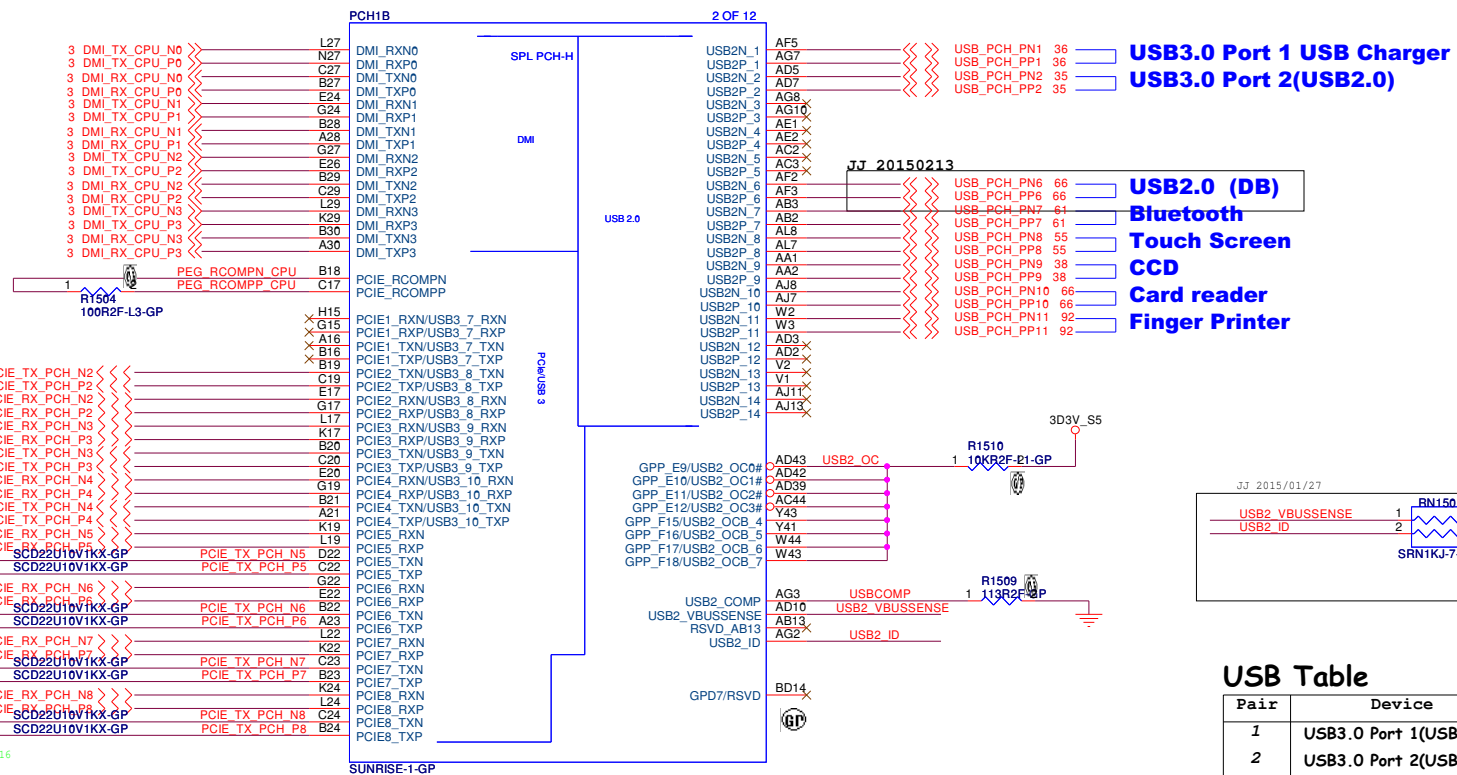
SSID = PCH

Alpine-Ridge

WIGIG

WIFI

LAN



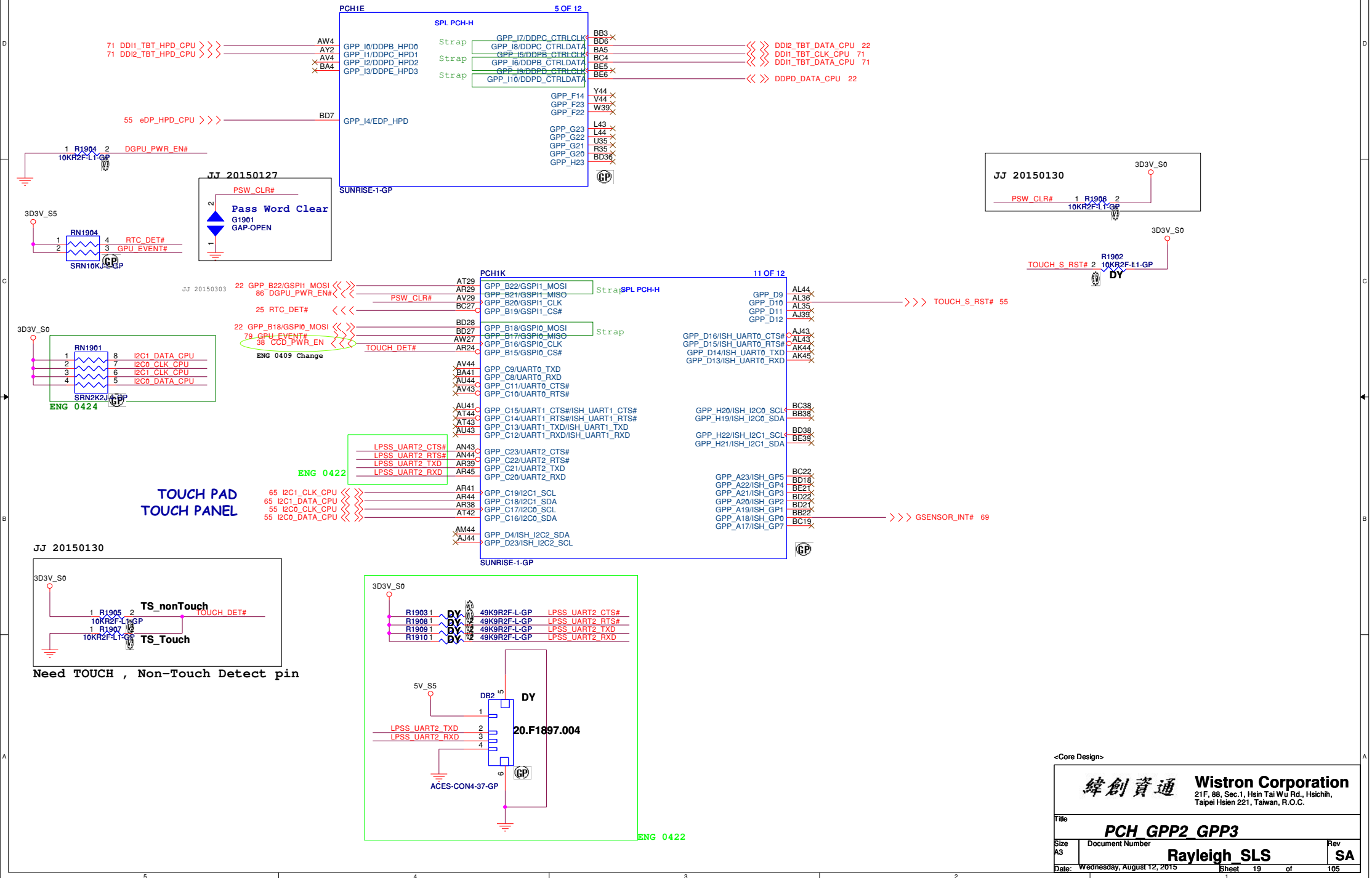
USB Table

Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	
4	
5	USB2.0
6	
7	Bluetooth
8	Touch Screen
9	CCD
10	Card reader
11	Finger Printer
12	
13	
14	

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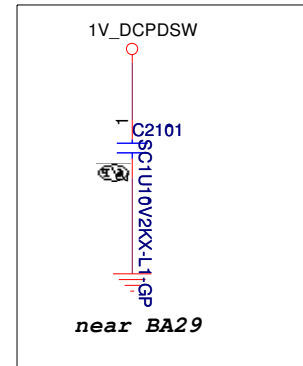
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH PCIE DMI USB	
Size A3	Document Number
Date: Wednesday, August 12, 2015	Rev SA
Rayleigh SLS	
Sheet 15 of 105	

SSID = PCH

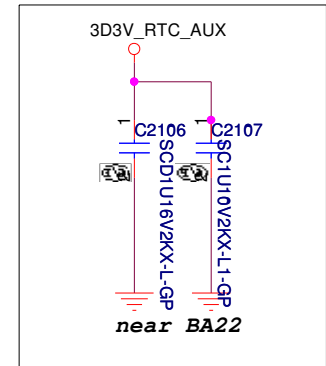


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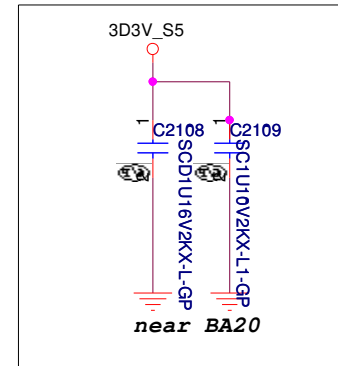
DcpDSW
1x 1uF



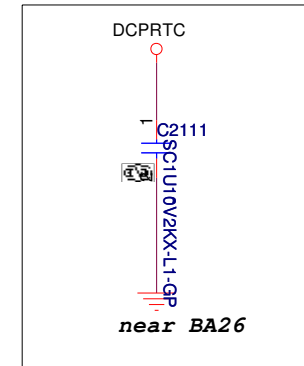
VccRTC
1x1 uF 1x0.1 uF



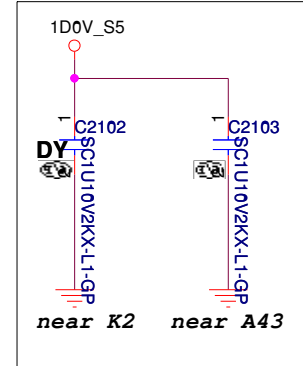
VccRTCPRIM
1x1 uF 1x0.1 uF



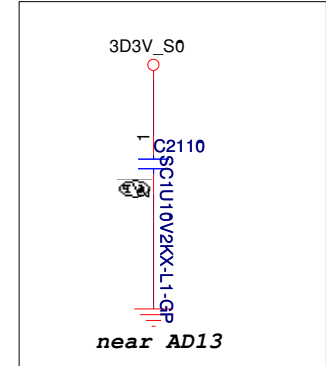
DcpRTC
1x 0.1uF



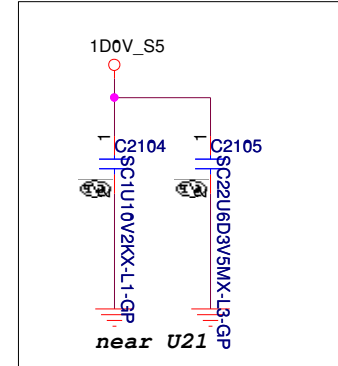
VccMPHYPLL / VccPCIE3PLL
1x1 uF



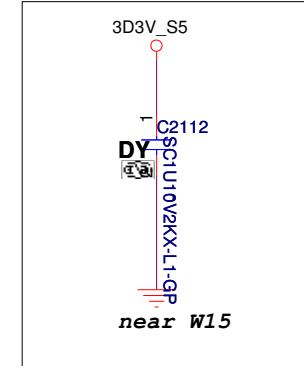
VccATS
1x1 uF



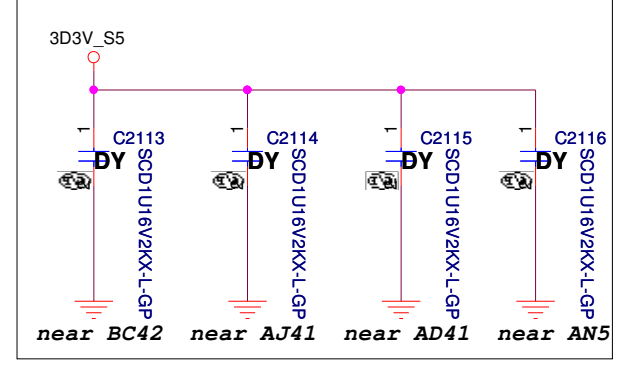
VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



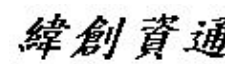
VccPGPPBCH / VccPGPPEF / VccPGPPG
/ VccPRIM
4x 0.1 uF



Decoupling and Power Connection Requirements for SKL 5/H PCH (DT / A10) (Sheet 1 of 2)							
Voltage Supply	Area	PCH Pins sharing area (ref)	Value	Size	Quantity	Placement type (R/through / S/Side)	Placement (ref)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V26, AC17, V28	1 uF 22 uF	0402 0805	1	E (<3 mm) E (<5 mm)	U21
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	1 uF	0402	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	1 uF	-	-	-	-
	VccUSB2PUL VccHDAPLL	A35, A35, AN19	-	-	-	-	-
	VccPRIM	AD22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	A320, A321, A323, A325	-	-	-	-	-
	VccPRIM	AA03, AA36, AA38, AC23, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
	V1.0B5 W	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	A341, AL41	0.1 uF	0402	1	E (<3 mm)	A341 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
	VccSPI	BE41, BE42, BE43	-	-	-	-	-
V1.8A/ V1.85/ V3.3S	VccPGPPD	BC44, BA45, BC45, BB45	-	-	-	-	-
	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
	VccHDA	BA15	-	-	-	-	-
V3.3A	VccRTCPRIM	BA20	1 uF 0.1 uF	0402 0402	1 1	E (<3 mm) E (<3 mm)	BA20
	VccPRIM	BD3, BE3, BE4	-	-	-	-	-
V3.3RTC	VccRTC	BA22	1 uF 0.1 uF	0402 0402	1 1	E (<5 mm) E (<3 mm)	BA22
	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
V3.3DS W	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

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Title

PCH_POWER_CAP1

Size A4





Document Number


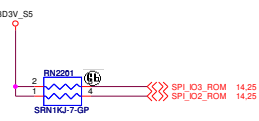



Rayleigh_SLS

Rev SA

Date: Wednesday, August 12, 2015

Sheet 21 of 105

Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic	Pull up at p.71 RN7101 						
High	Detected	Detected	Detected	Enable	LPC	Disable	1:SLAVE ATTACEHD FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confidentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23 / PCHHOT#
Schematic								
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

[H,S,U,Y] Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update

The current Skylake Platform Design Guide (PDG) states that a 1 K pull-up resistor is required on the **PCH SPI_IO2 and SPI_IO3 signals**.

This 1K pull up resistor is no longer needed on Skylake platform and can be removed from the motherboard. The new guidelines will be updated in a future release of the Skylake PDG.

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File		PCH_STRAP	
Size	Document Number	Rev	
A2	Rayleigh_SLS	SA	
Date	Wednesday, August 12, 2015	Sheet	22 of 105

SSID = PCH

PCH1I 9 OF 12

SPL PCH-H

PCH1L 12 OF 12

SPL PCH-H

PCH1J 10 OF 12

SPL PCH-H

AR22
W13
U13
P31
N31
P27
R27
N29
P29
AN29
R24
P24
AT3
AT4
AY5
AL2
AK1
XDP_FREQ# 6.99
XDP_PRDY# 6.99
PROC_TRST# 6.99
PCH_2_CPU_TRIGGER 8
CPU_2_PCH_TRIGGER 8

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Title PCH_RSVD_VSS
Size B Document Number Rayleigh_SLS Rev SA
Date: Wednesday, August 12, 2015 Sheet 23 of 105

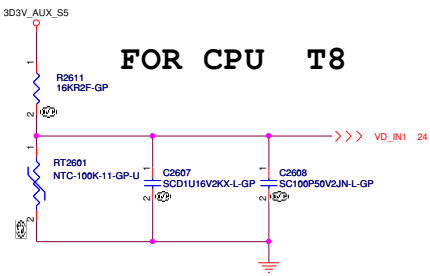
SSID = Thermal

ADB (Active Dusting Blower) function

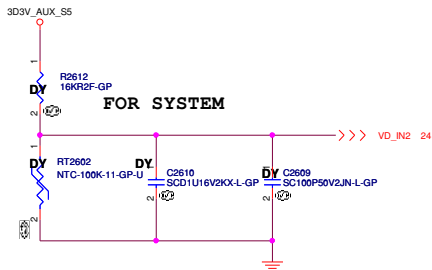
AFTP TESTPOINT

FAN_TACH1_C >>> FAN_TACH1_C 89
FAN_TACH2_C >>> FAN_TACH2_C 89

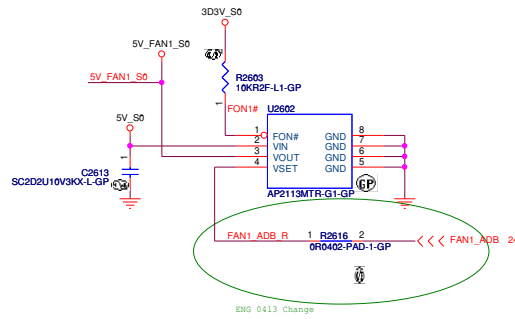
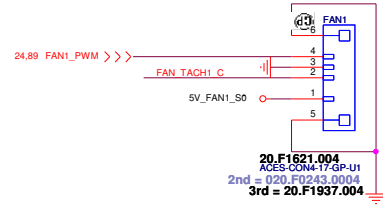
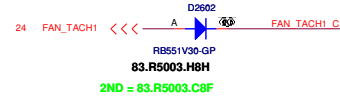
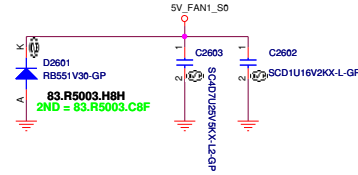
FOR CPU T8



FOR SYSTEM



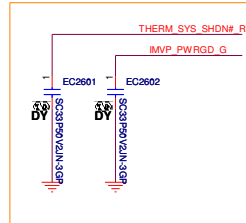
Layout 15 mil



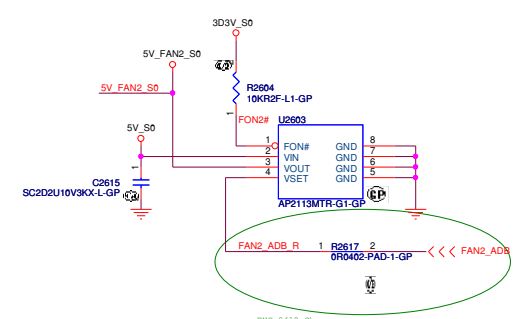
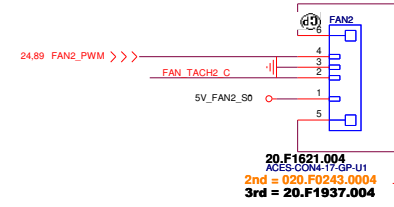
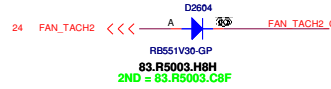
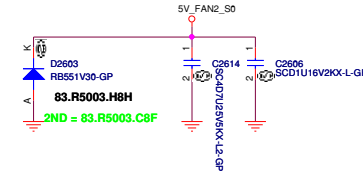
ENG 0413 Change

T8 = 85 degree

EMI Reserved

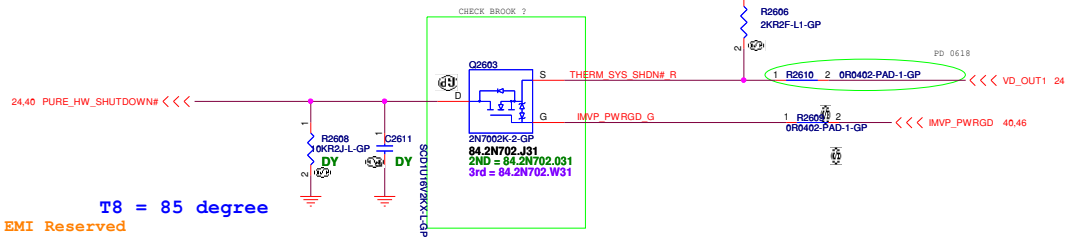


Layout 15 mil



ENG 0410 Change

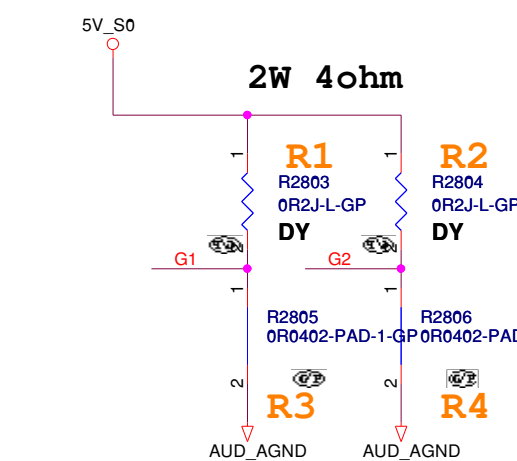
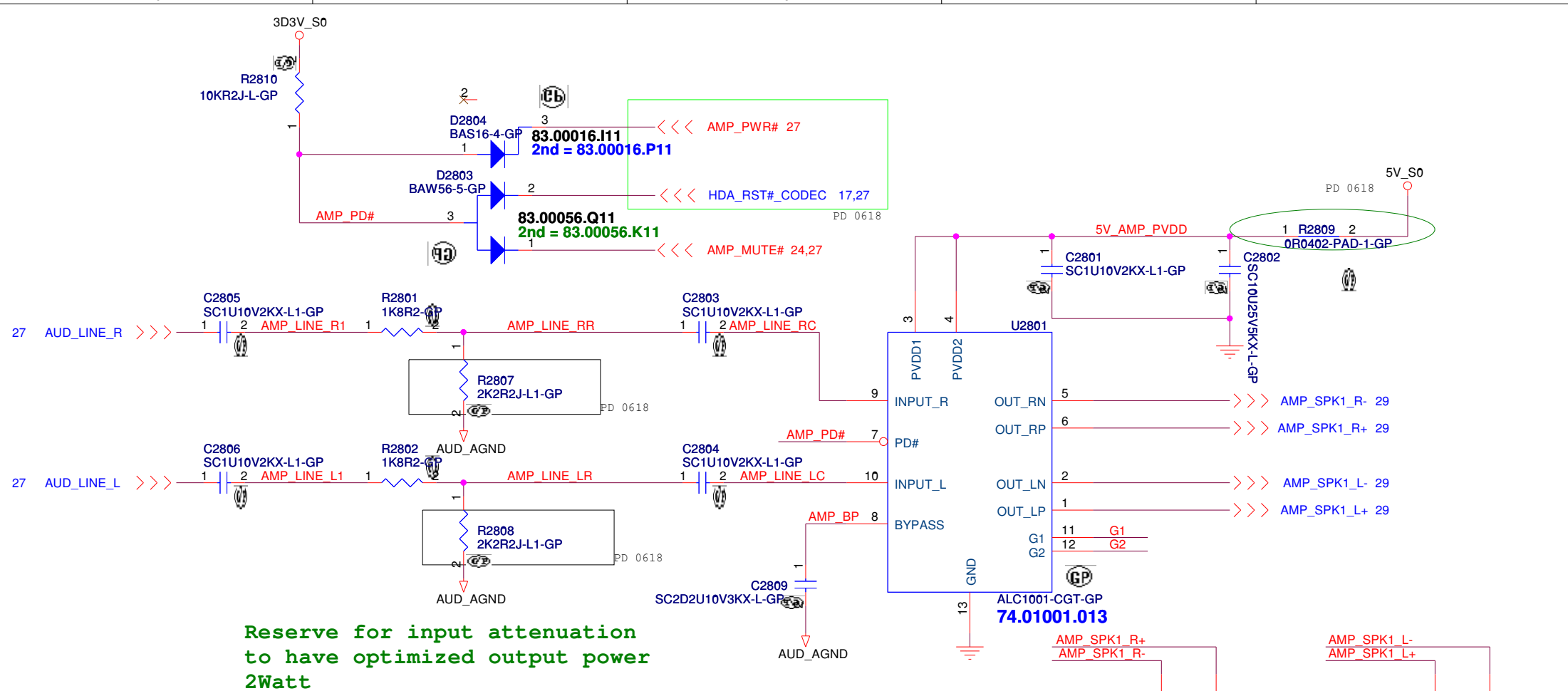
CHECK BROOK ?



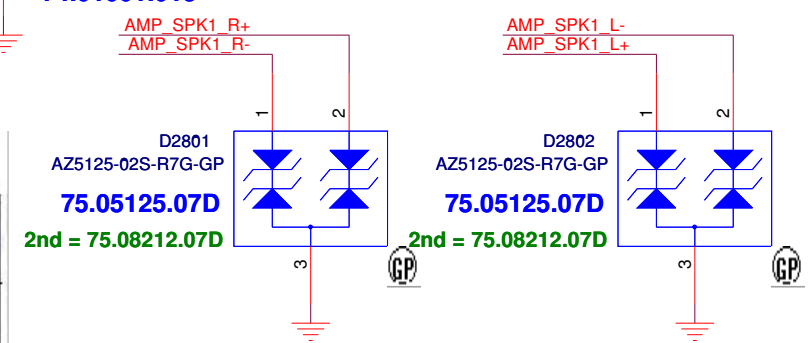
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File Thermal T8 and FAN
Size Document Number
Custom Rayleigh SLS
Date: Wednesday, August 12, 2015 Sheet 26 of 105



Output Gain Table				
R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



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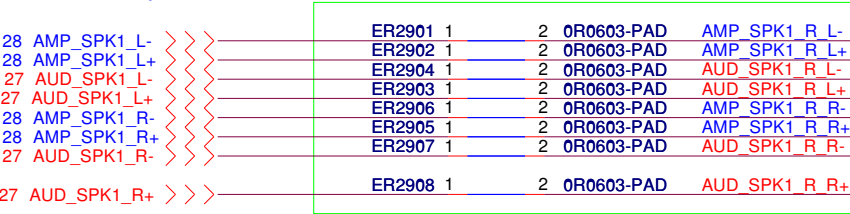
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Title: **(Reserved)**

Size A4	Document Number Rayleigh SLS	Rev SA
Date: Monday, September 07, 2015	Sheet 28 of 105	

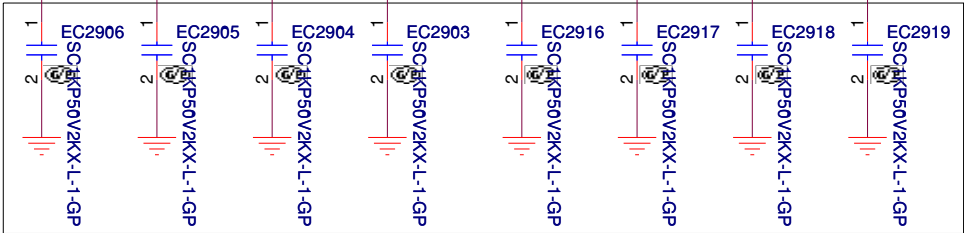
SSID = AUDIO

Speaker

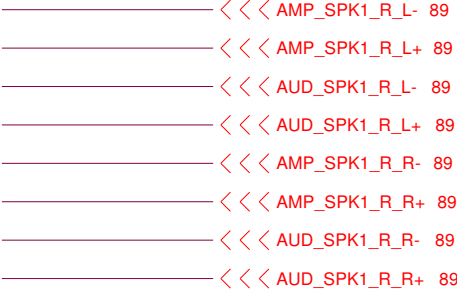
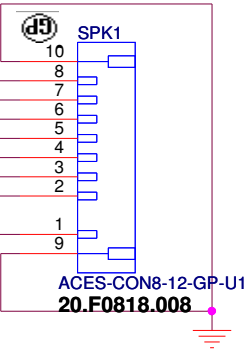


PD JJ 0625

Layout Note:
Trace width=40mil



0513-SC Anthony



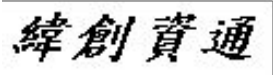
AFTP TESTPOINT

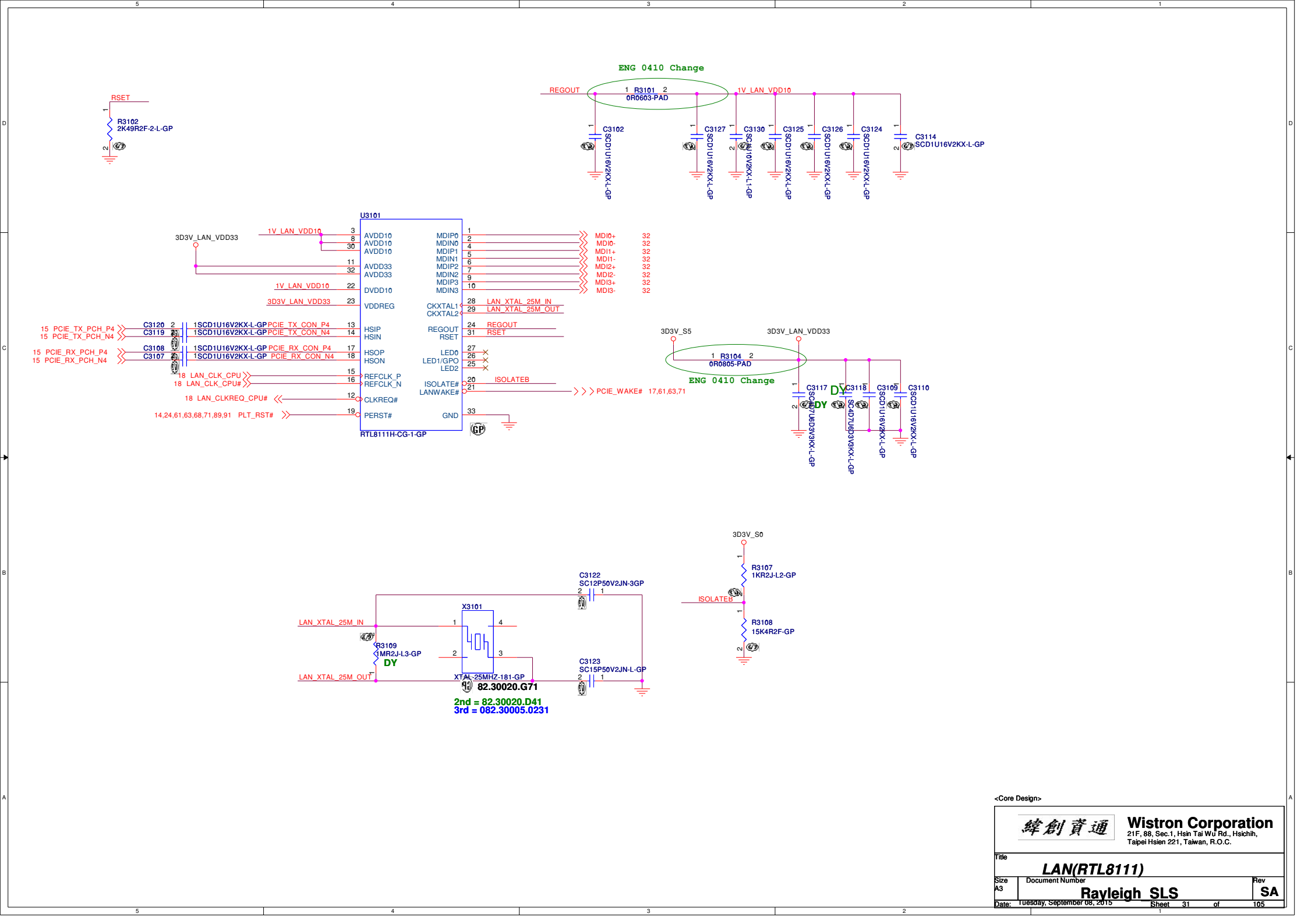
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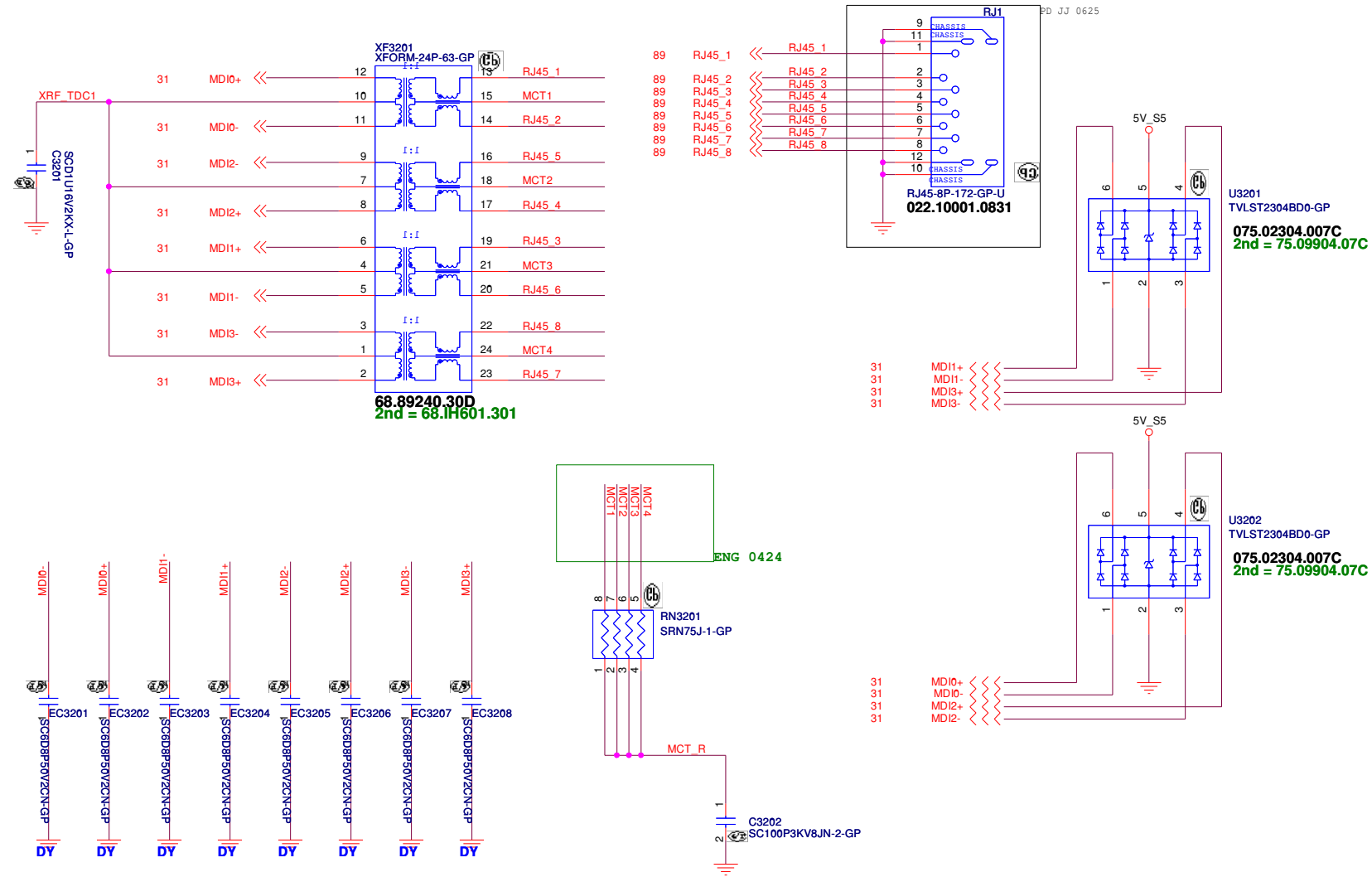
Title			Speaker/ALC255	
Size	Document Number		Rev	
A4	Rayleigh SLS		SA	
Date:	Wednesday, August 12, 2015		Sheet 29	of 105

5	4	3	2	1
D				D
C				C
B				B
A			<Core Design> <div><div></div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div> <div><div>Title</div><div>(Reserved)</div></div> <div><div>Size A</div><div>Document Number Rayleigh_SLS</div><div>Rev SA</div></div> <div><div>Date: Wednesday, August 12, 2015</div><div>Sheet 30 of 105</div></div>	A



<Core Design>

SSID = LAN



<Core Design>

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Title

RJ45+Transformer

Size
B

Document Number

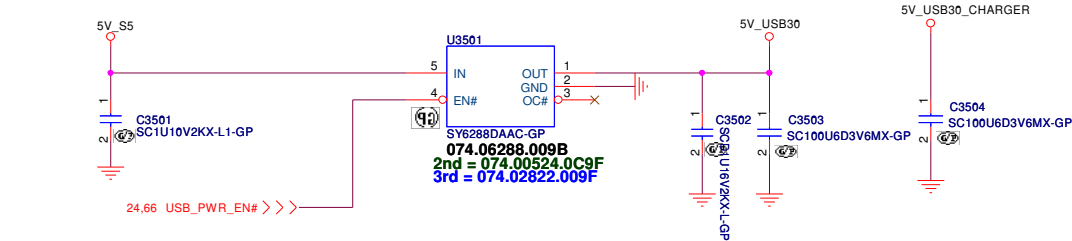
Rev
SA

Rayleigh SLS

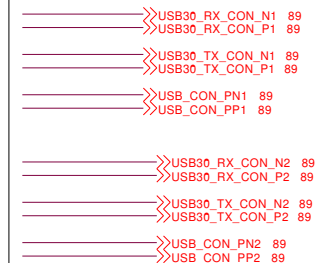
Date: Wednesday, August 12, 2015

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Low Active 2A

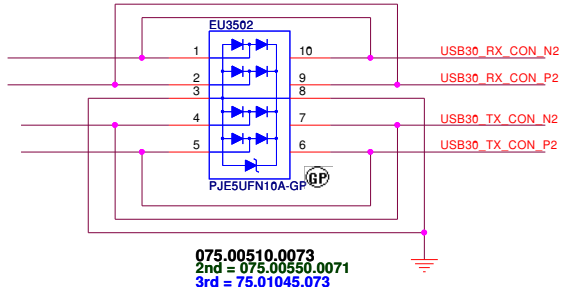
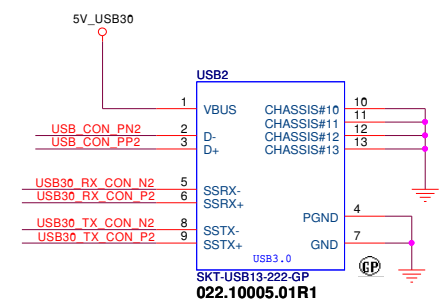
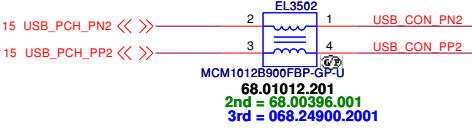
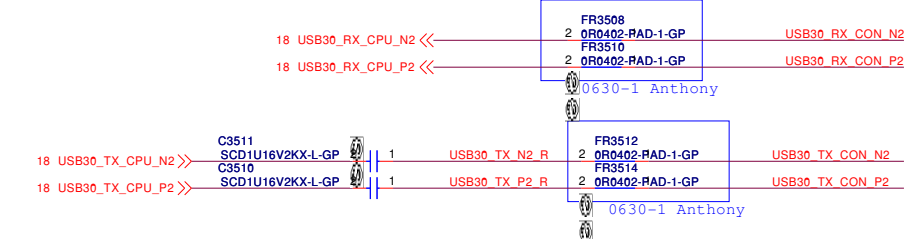
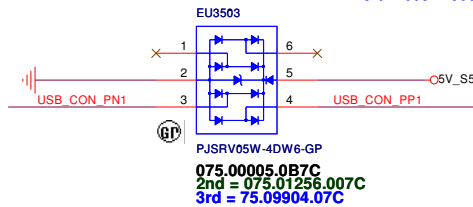
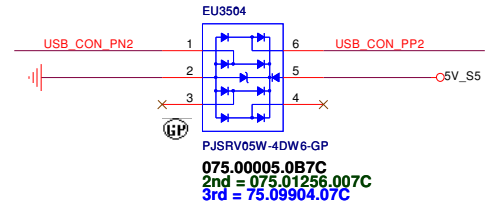
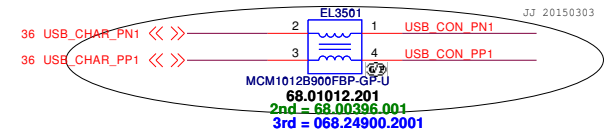
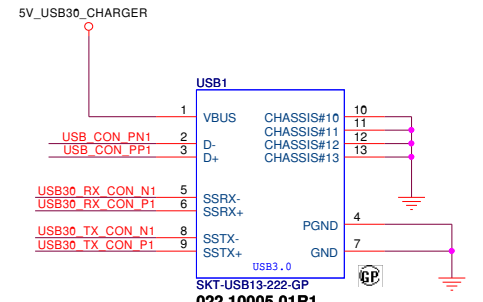
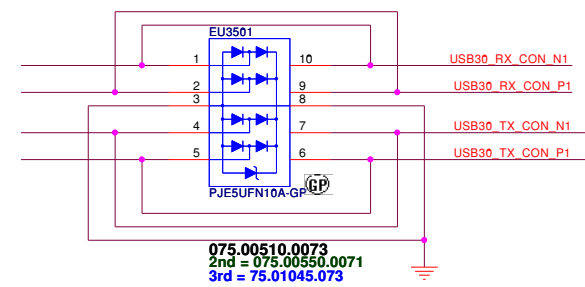
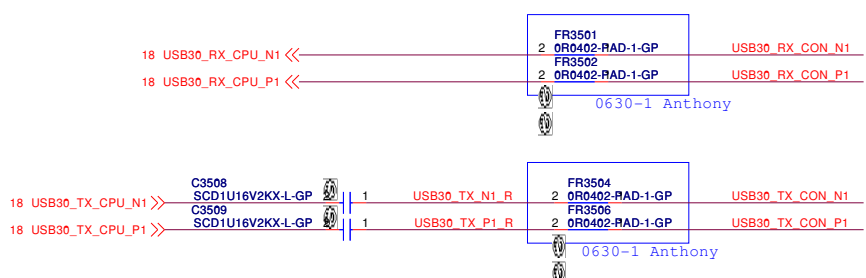


AFTP TESTPOINT



USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



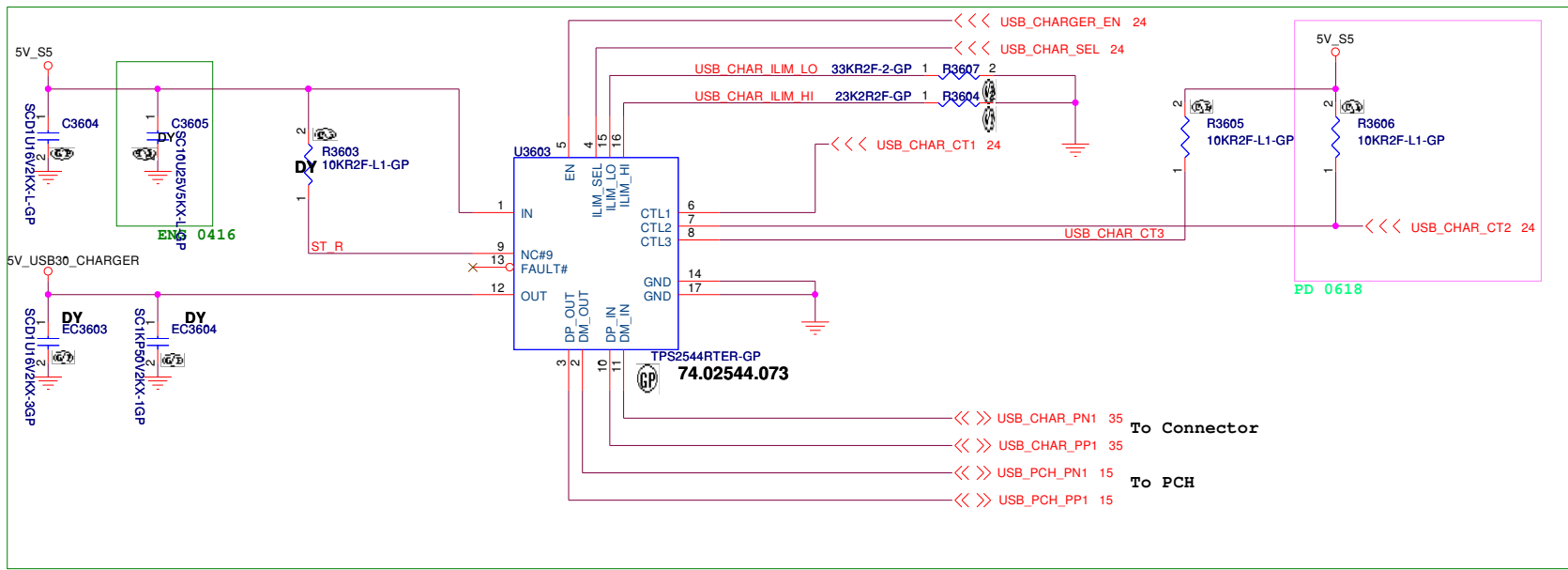
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Title **USB3.0 CONN**

Size A3 Document Number **Rayleigh SLS** Rev **SA**

Date: Wednesday, August 12, 2015 Sheet 35 of 105



ENG 0413 Change

Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1 Charging mode
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

<Core Design>

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Title

USB CHARGER

Size B

Document Number

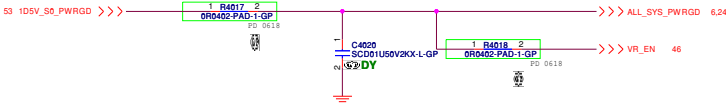
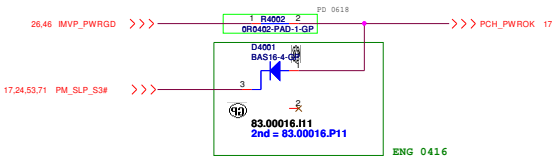
Rayleigh SLS

Rev SA

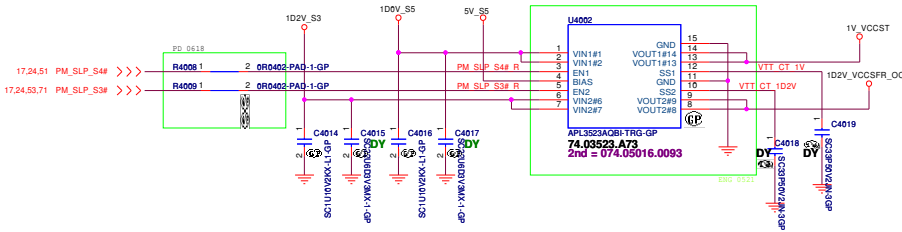
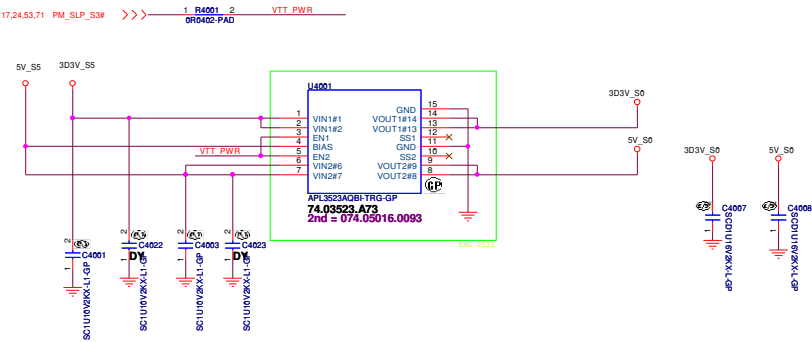
Date: Wednesday, August 12, 2015

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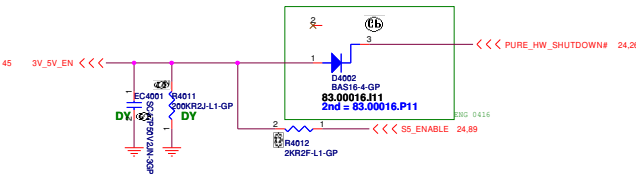
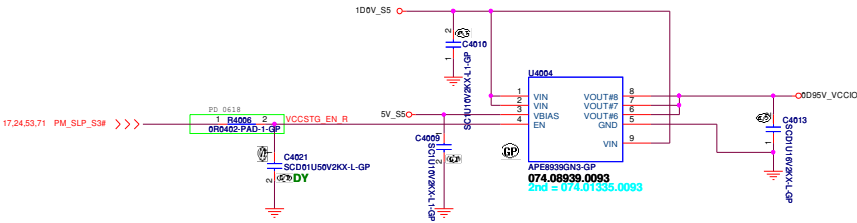
Power Sequence



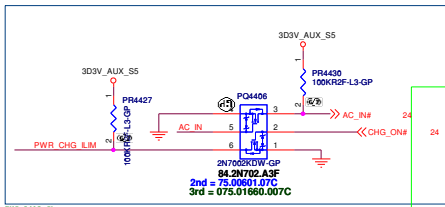
ANNIE Run Power



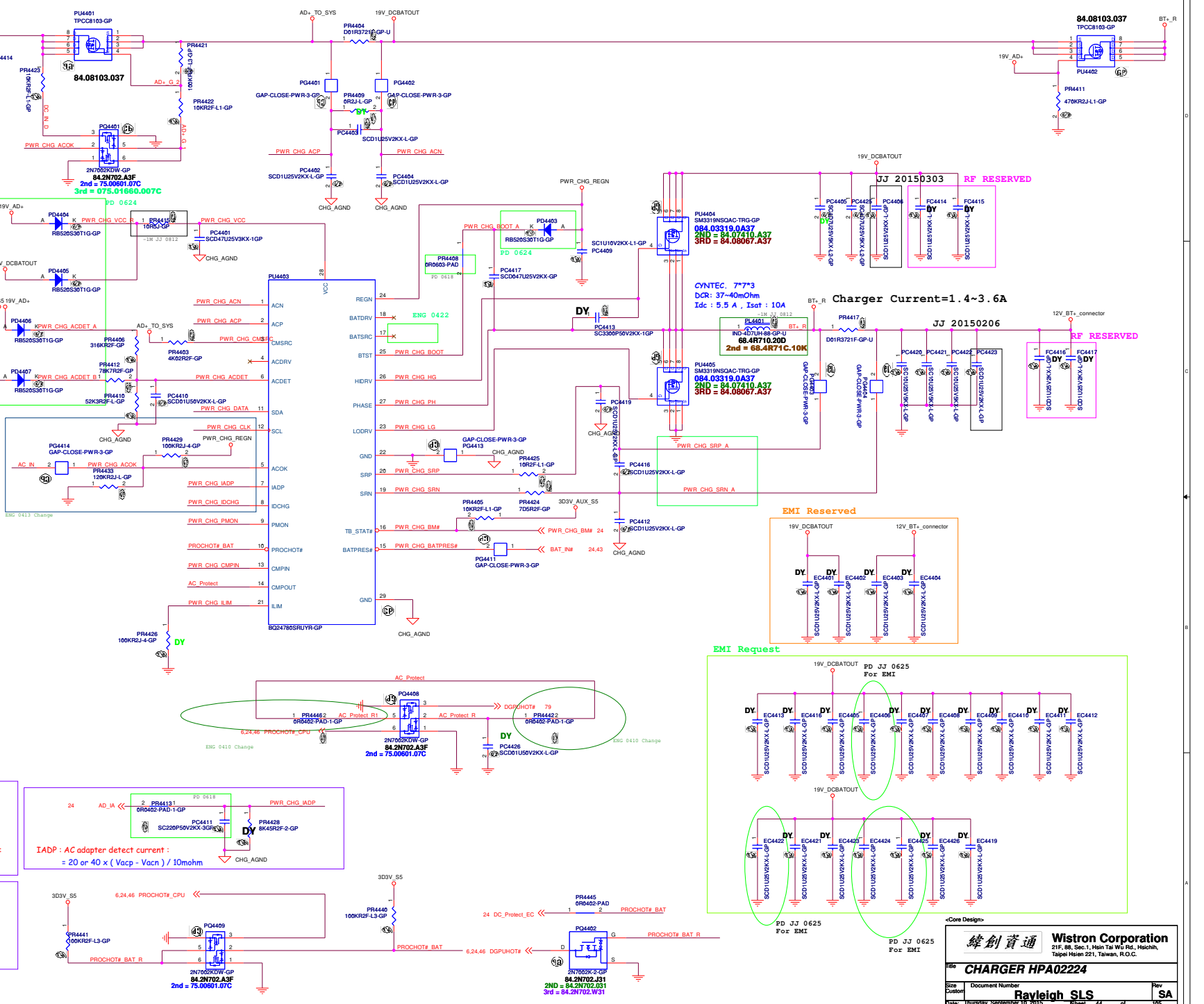
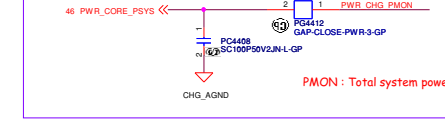
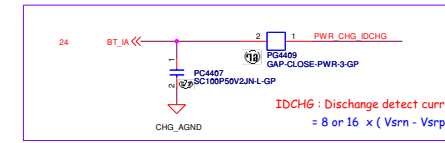
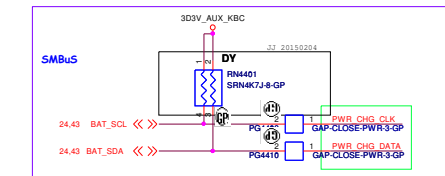
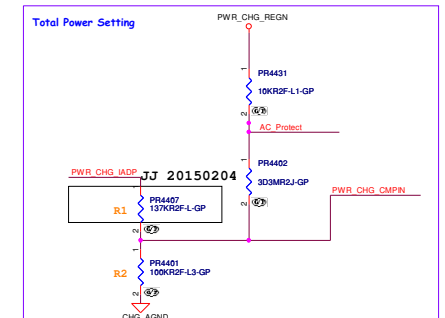
JJ 20150305

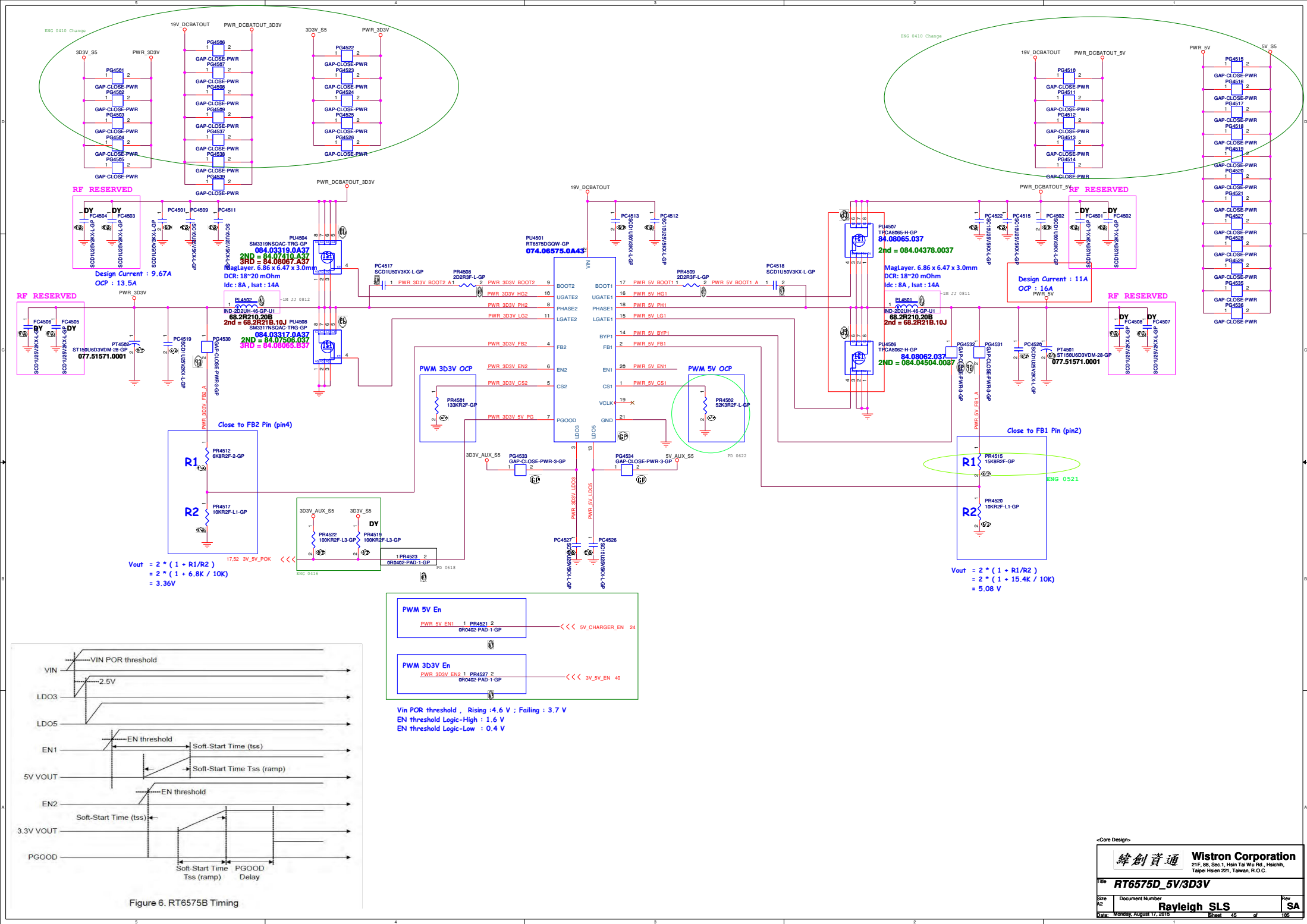


SSID = Charger



Adaptor	Protect	Sense	Amplifier	R1	R2
135.00 W	6.92 A	102%	7.06 A	10 m Ohm	40
120.00 W	6.15 A	102%	6.28 A	10 m Ohm	40
90.00 W	4.02 A	102%	4.71 A	10 m Ohm	40





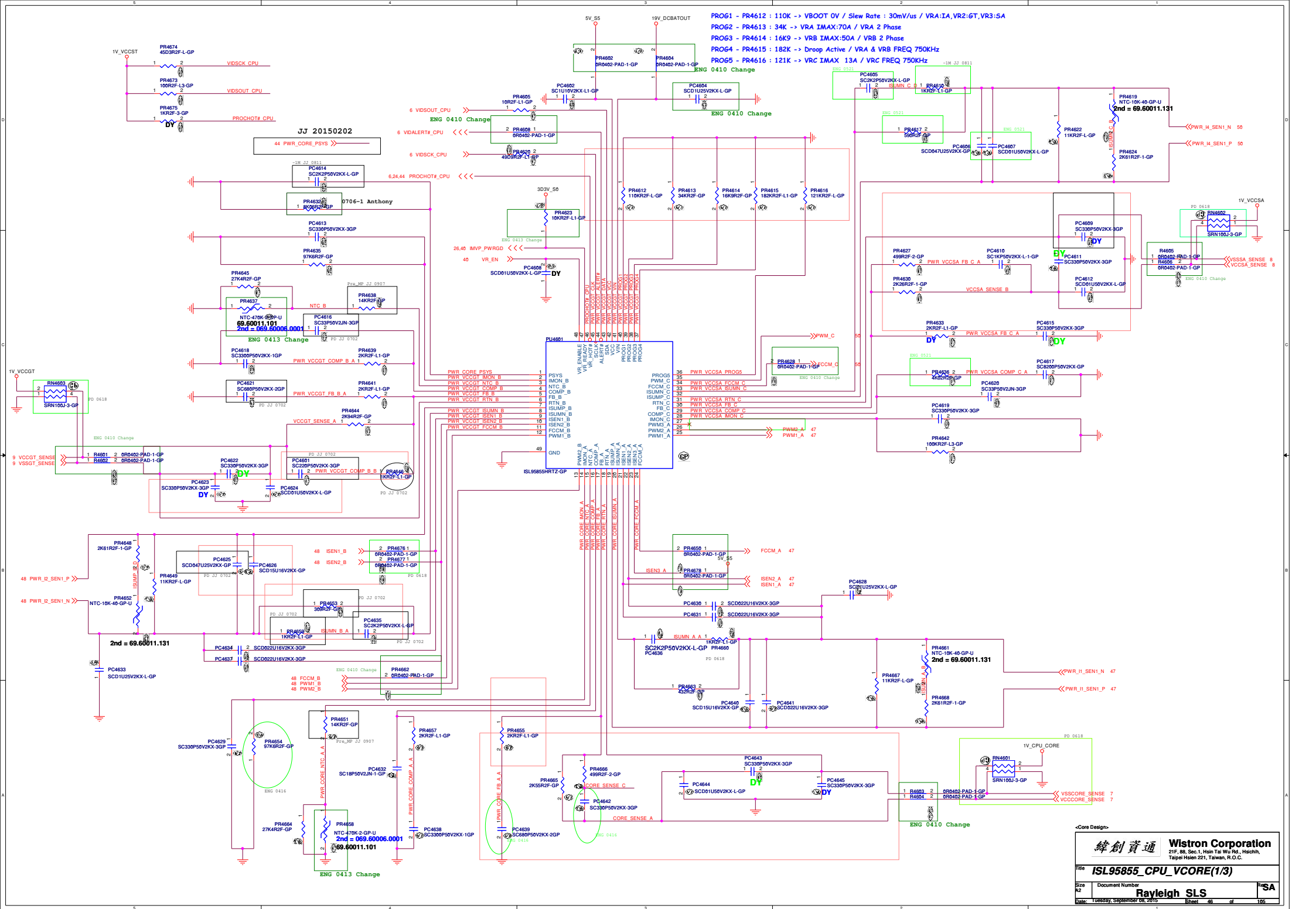
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緯創資通

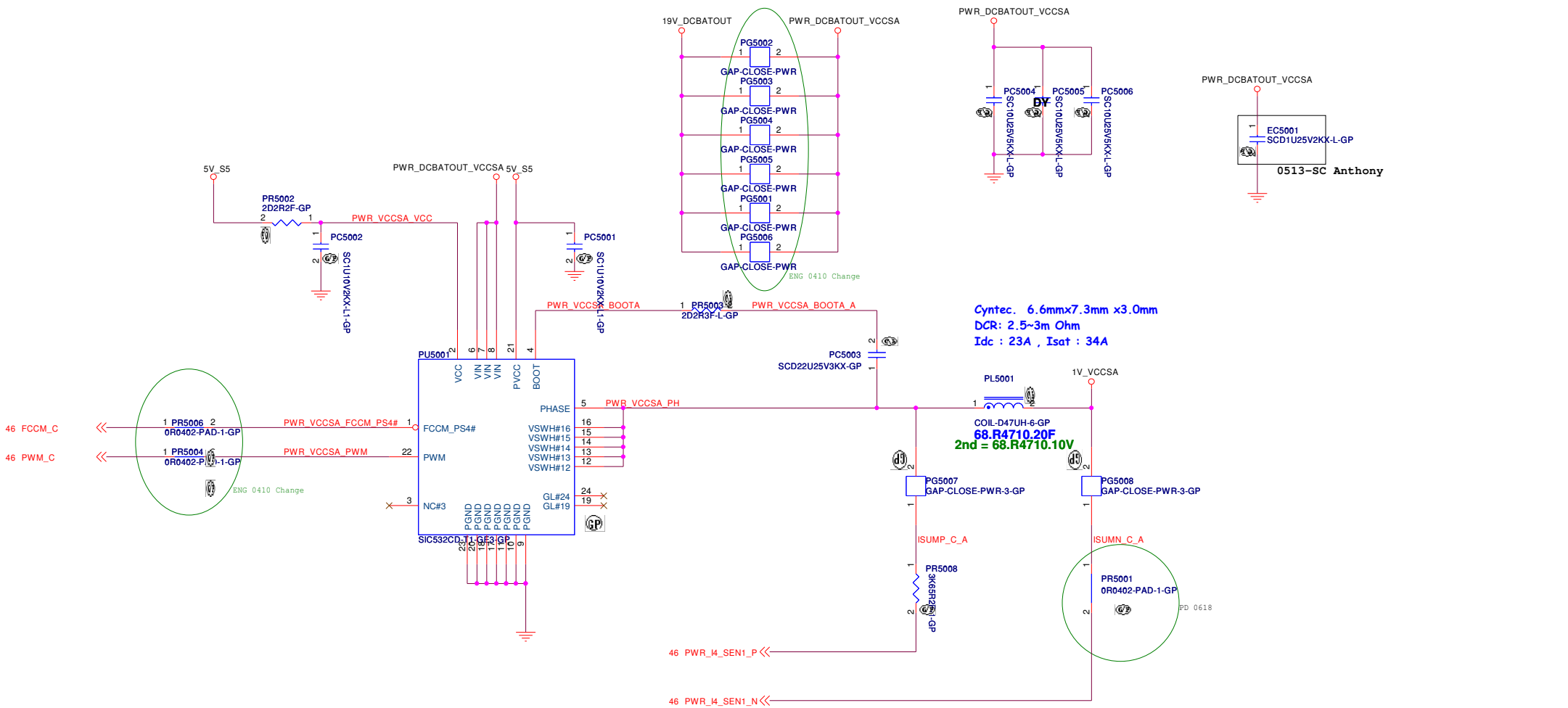
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File **RT6575D_5V/3D3V**

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PROG1 - PR4612 : 110K -> VBOOT OV / Slew rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz



<Core Design>

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File

SIC631CD VCCSA

Size
A3

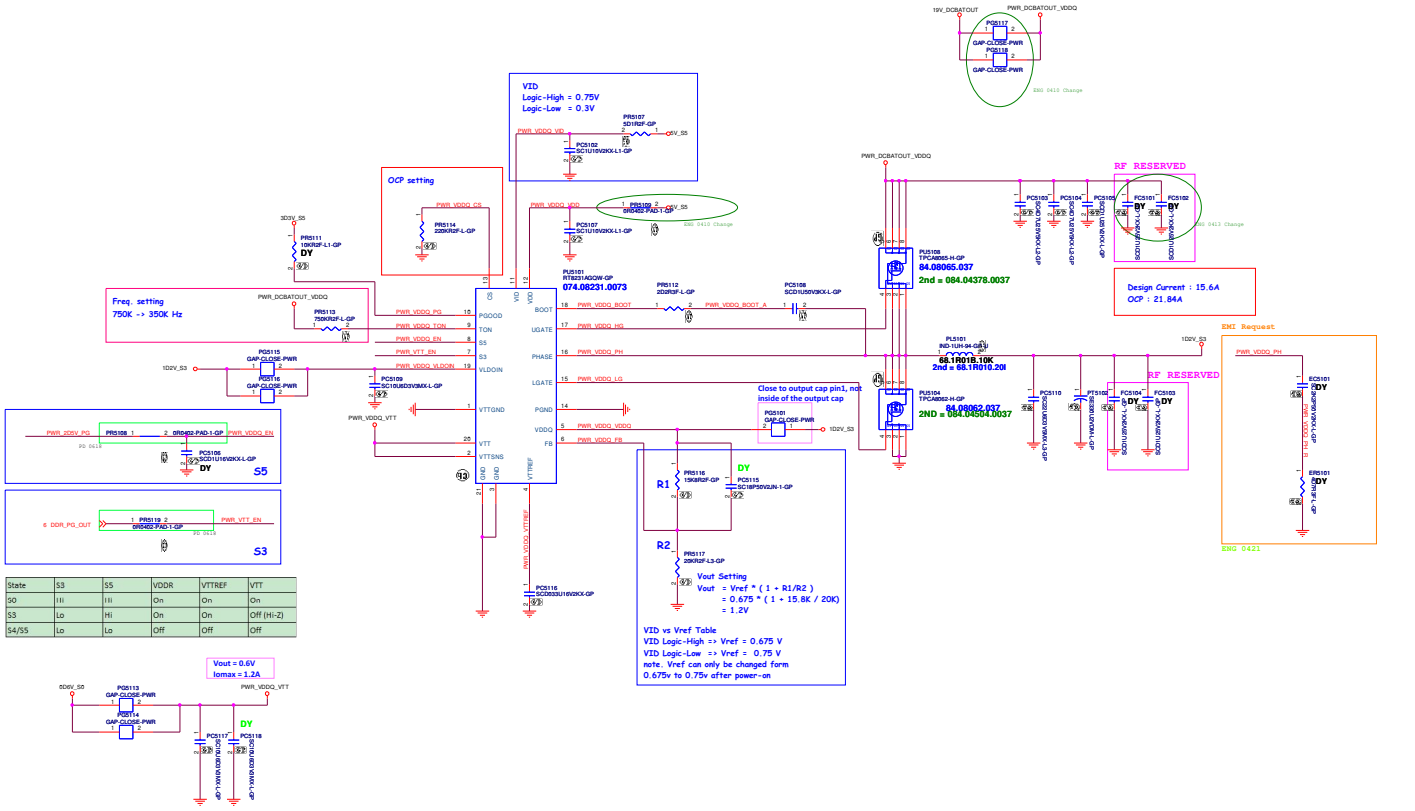
Document Number

Rayleigh SLS

Rev
SA

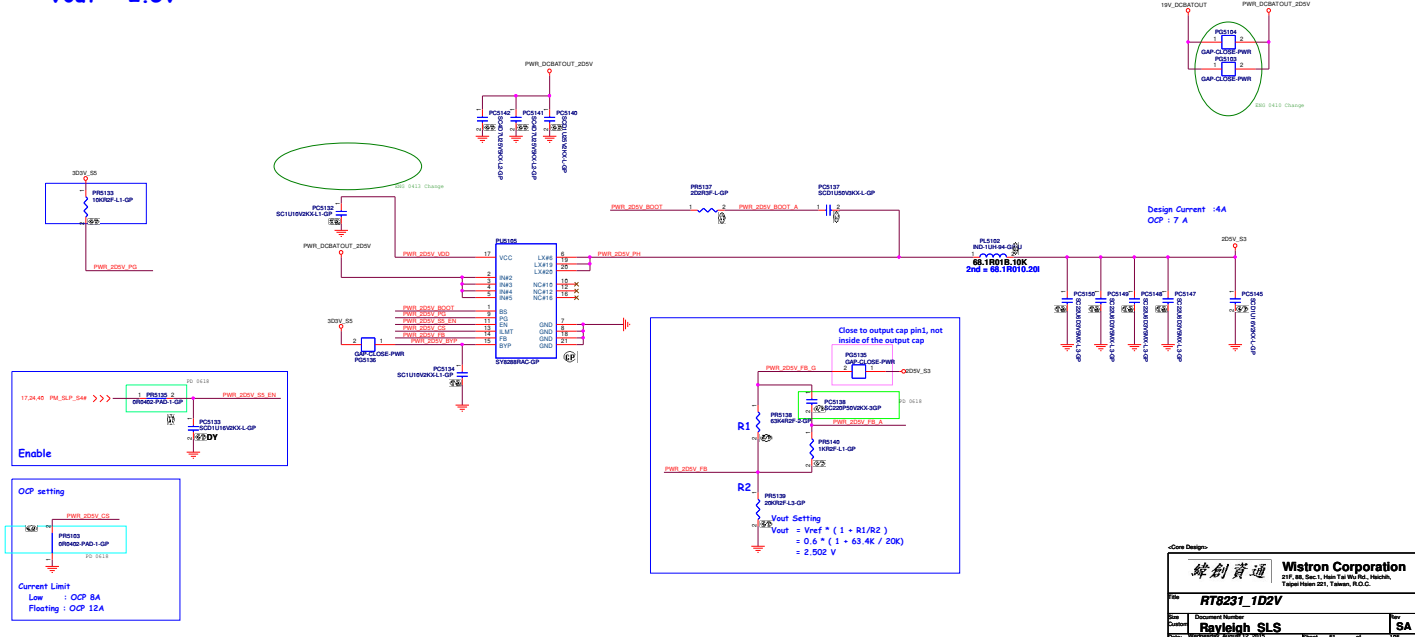
Date: Wednesday, August 12, 2015

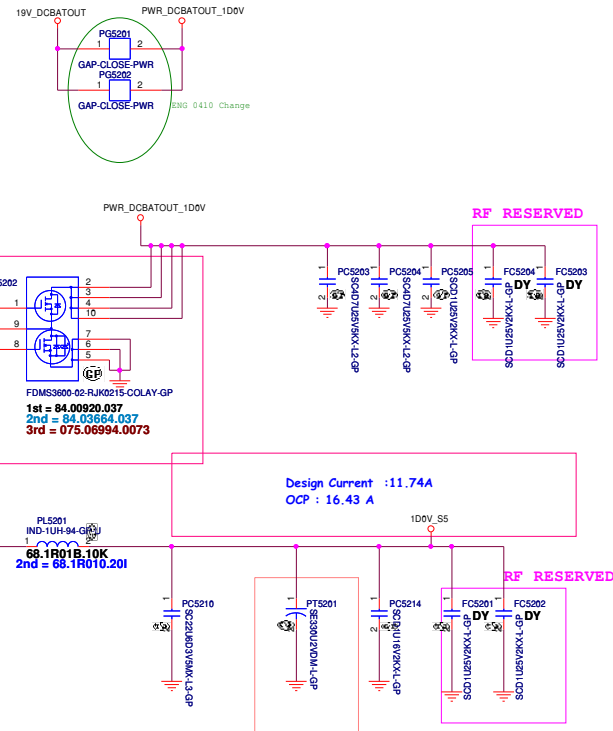
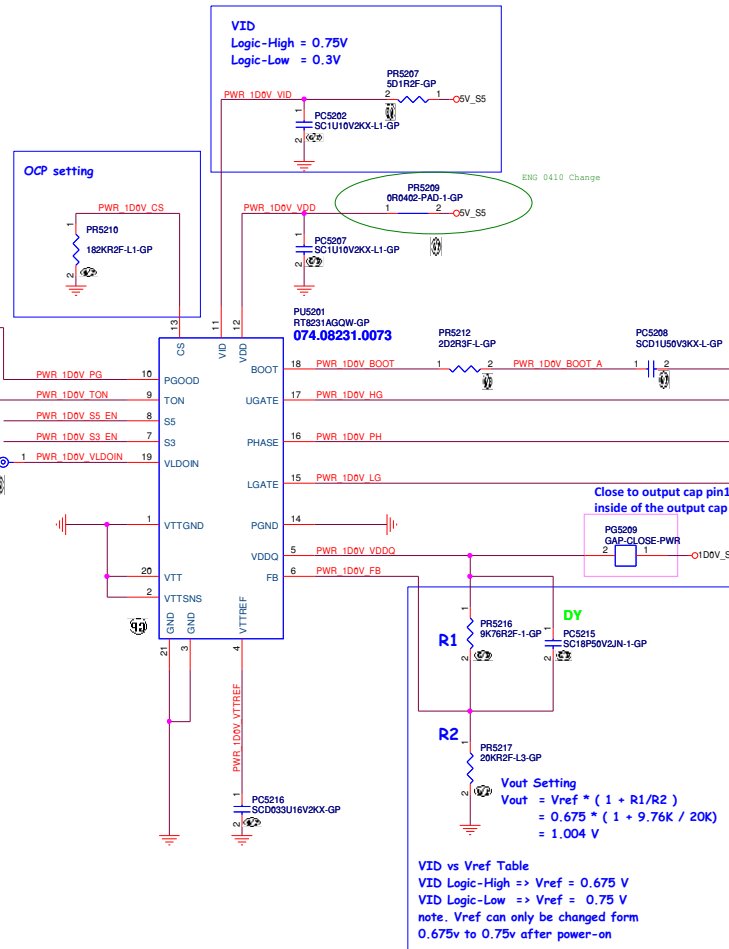
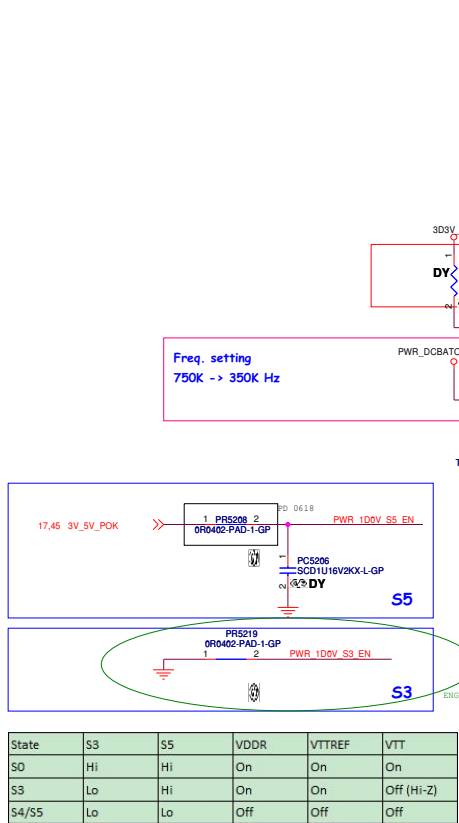
Sheet 50 of 105

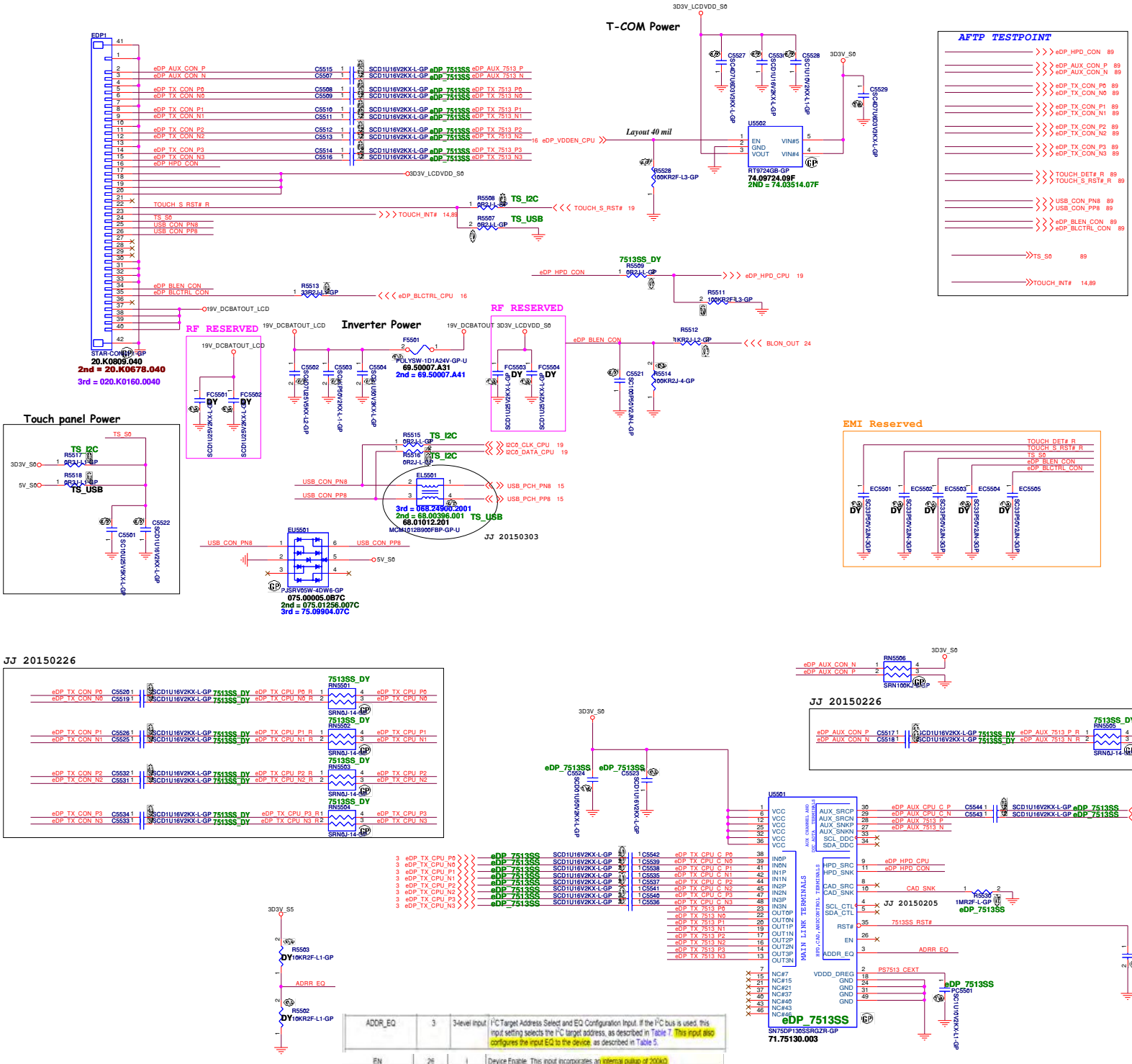


SY8288 For DDR4

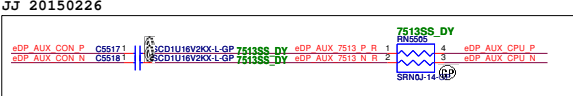
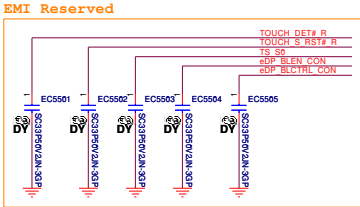
Vout = 2.5V







AFTP TESTPOINT	
>>> eDP_HPDCON	89
>>> eDP_AUXCON_P	89
>>> eDP_AUXCON_N	89
>>> eDP_TXCON_P0	89
>>> eDP_TXCON_N0	89
>>> eDP_TXCON_P1	89
>>> eDP_TXCON_N1	89
>>> eDP_TXCON_P2	89
>>> eDP_TXCON_N2	89
>>> eDP_TXCON_P3	89
>>> eDP_TXCON_N3	89
>>> TOUCH_DET#_R	89
>>> TOUCH_RST#_R	89
>>> USB_CON_PN8	89
>>> USB_CON_PP8	89
>>> eDP_BLENCON	89
>>> eDP_BLCCTRLCON	89
>>> TS_S0	89
>>> TOUCH_INT#	14.89



ADDER_EQ	
EN	26
Device Enable	This input incorporates an internal pullup of 250kΩ

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

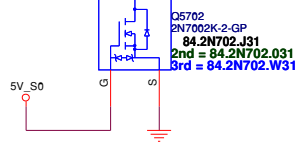
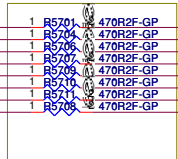
71 HDMI_CLK_CON_N3 >>>
71 HDMI_CLK_CON_P3 >>>
71 HDMI_DATA_CON_N0 >>>
71 HDMI_DATA_CON_P0 >>>

HDMI_CLK_CON_N3
HDMI_CLK_CON_P3
HDMI_DATA_CON_N0
HDMI_DATA_CON_P0

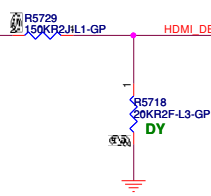
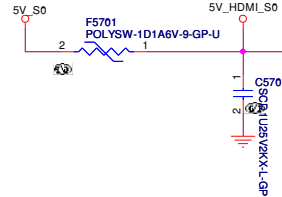
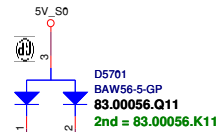
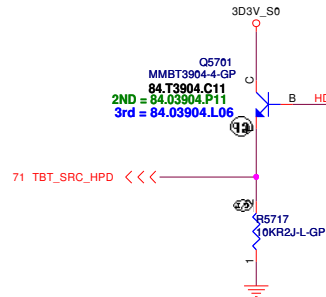
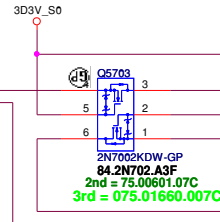
71 HDMI_DATA_CON_N1 >>>
71 HDMI_DATA_CON_P1 >>>
71 HDMI_DATA_CON_N2 >>>
71 HDMI_DATA_CON_P2 >>>

HDMI_DATA_CON_N1
HDMI_DATA_CON_P1
HDMI_DATA_CON_N2
HDMI_DATA_CON_P2

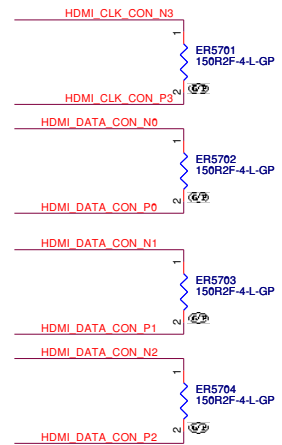
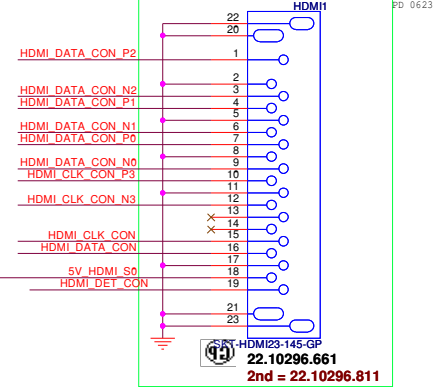
Check ok before ENG



71 TBT_HDMI_DDC_CLK >>>
71 TBT_HDMI_DDC_DATA >>>



HDMI CONN



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Title			HDMI Level Shifter/Conn	
Size	Document Number			Rev
Custom		Rayleigh SLS		SA
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SSID = SATA

SATA HDD Connector

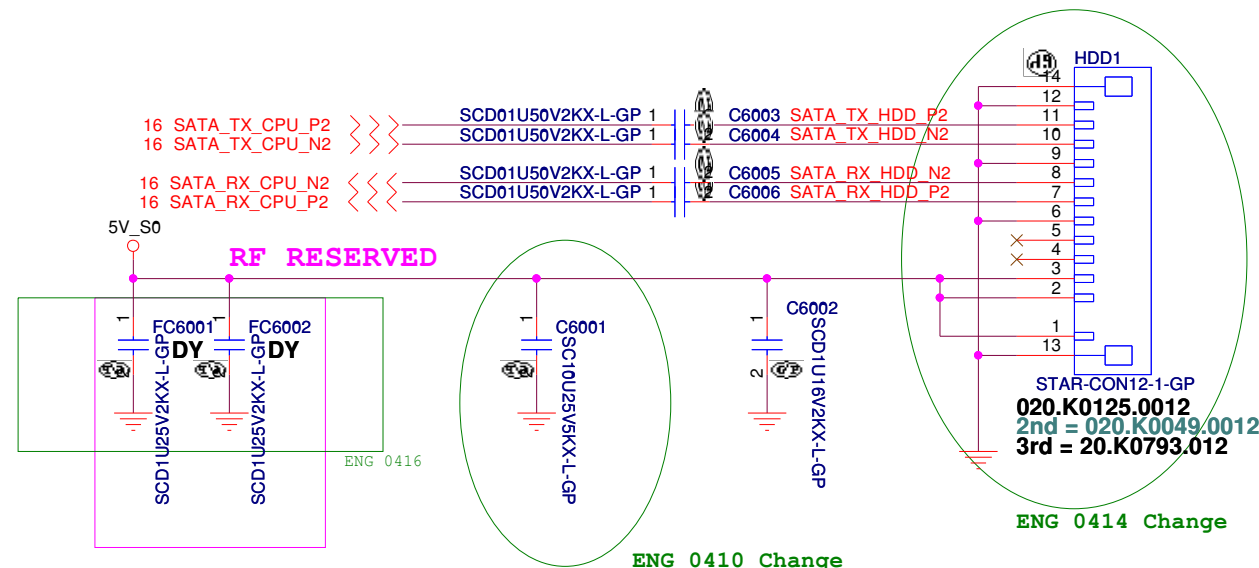
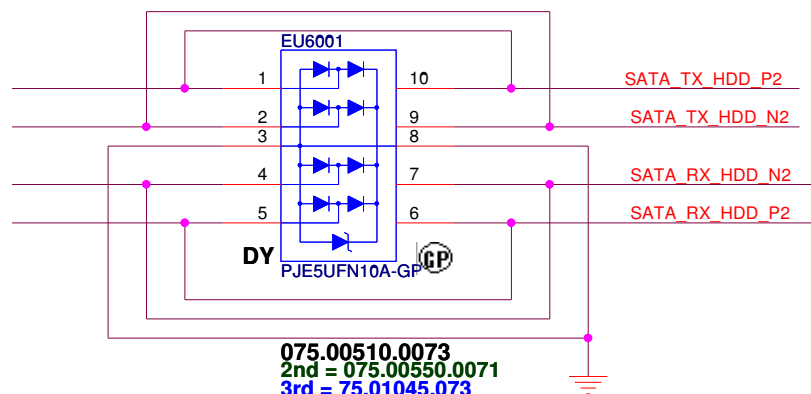
AFTP TESTPOINT

```

89 SATA_TX_HDD_P2  >>> _____
89 SATA_TX_HDD_N2  >>> _____

89 SATA_RX_HDD_N2  <<< _____
89 SATA_RX_HDD_P2  <<< _____

```



AC coupling caps near connector < 100 mils

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Title

HDD/ODD

Size

Document Number

Rev

Rayleigh SLS

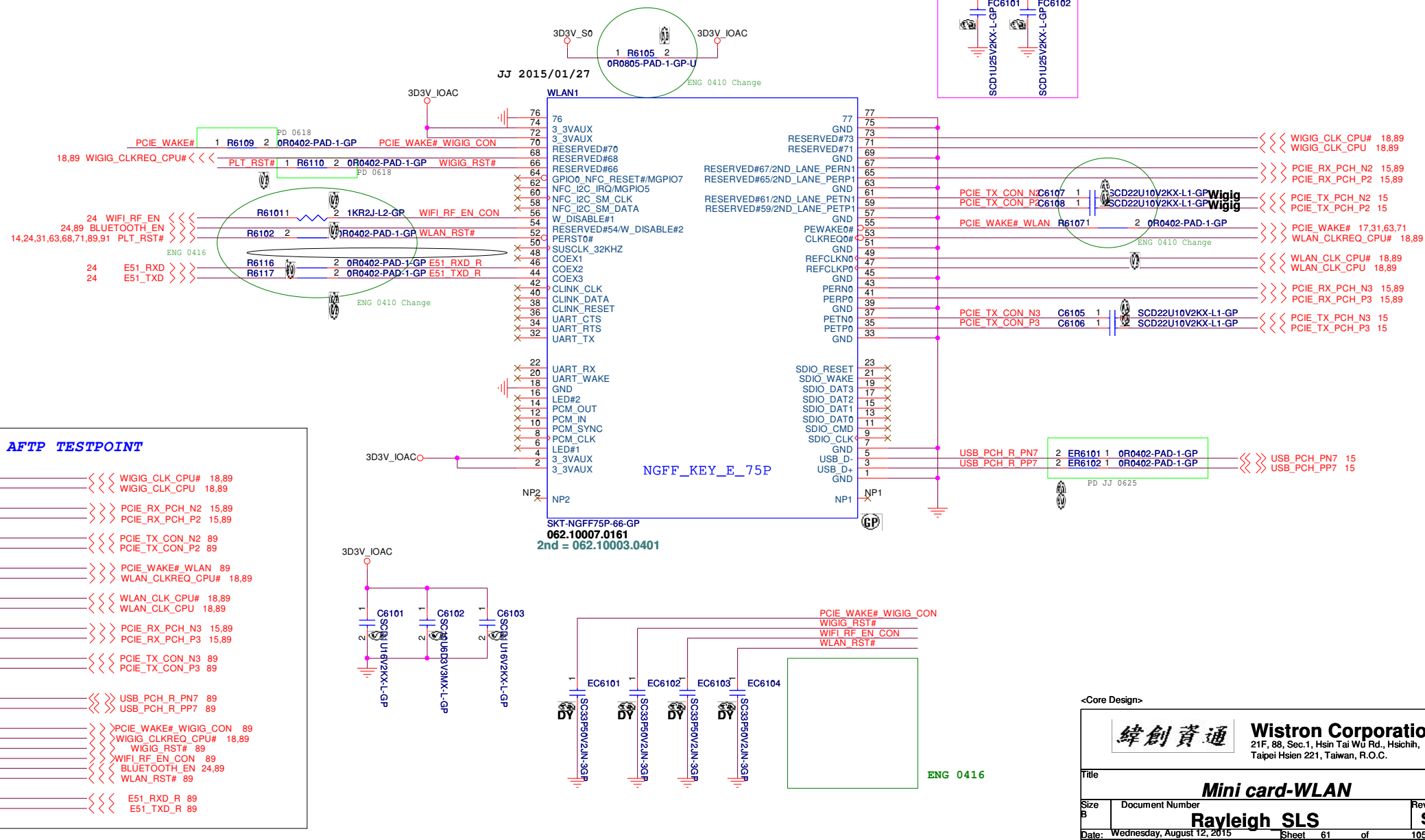
SA

Date: Wednesday, August 12, 2015

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SSID = Wireless/ Wigig

NGFF Connector (802.11a/b/g/n)



<Core Design>

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Title

Mini card-WLAN

Size

Document Number

Date

Wednesday, August 12, 2015

Sheet

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of

105

Rev

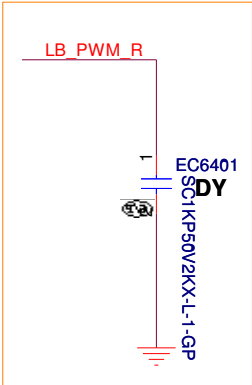
SA

Rayleigh SLS

SA

SSID = User.Interface

EMI Reserved

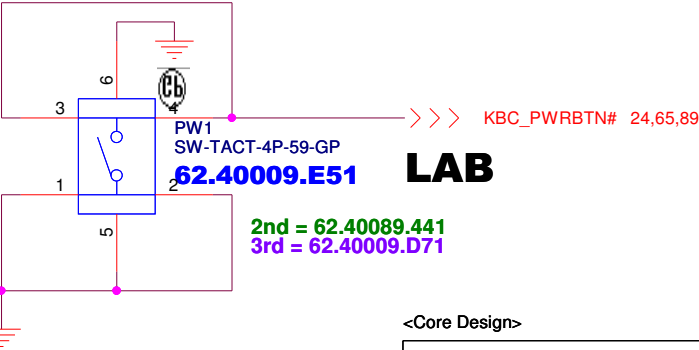
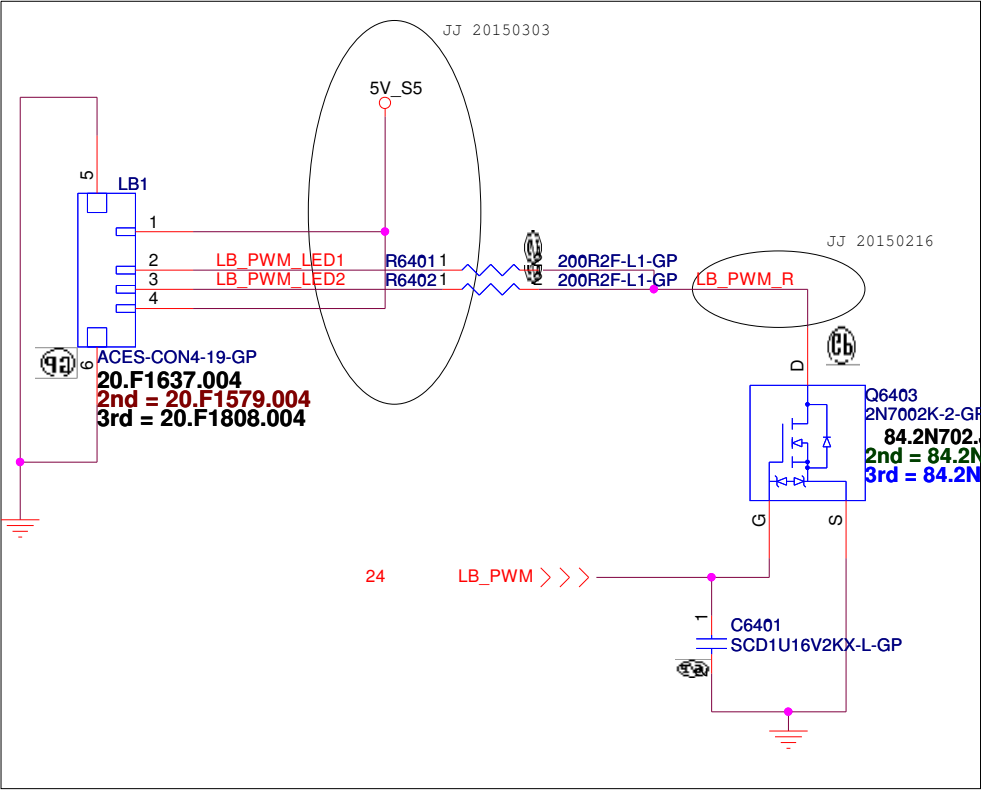


ENG 0422

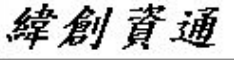
AFTP TESTPOINT

89 LB_PWM_LED1 >>> _____
89 LB_PWM_LED2 >>> _____

Power Button

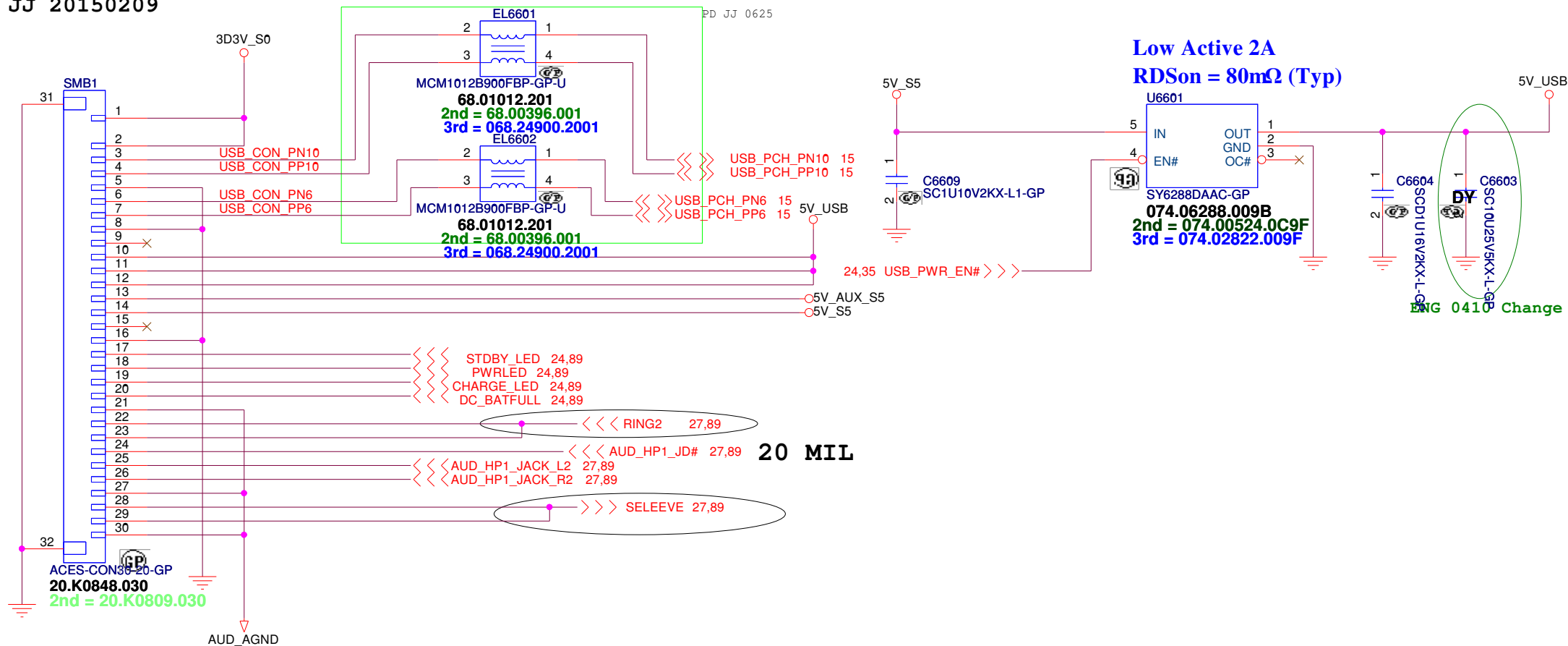


<Core Design>



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Title		
LED Bard/Power Button		
Size	Document Number	Rev
A4	Rayleigh_SLS	SA
Date:	Tuesday, September 08, 2015	Sheet 64 of 105



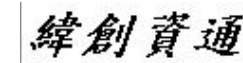
AFTP TESTPOINT

```

89 USB_CON_PN10 > > > _____
89 USB_CON_PP10 > > > _____
89 USB_CON_PN6  > > > _____
89 USB_CON_PP6  > > > _____

```

<Core Design>



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Title

IO Board Connector

Size
A4

Document Number

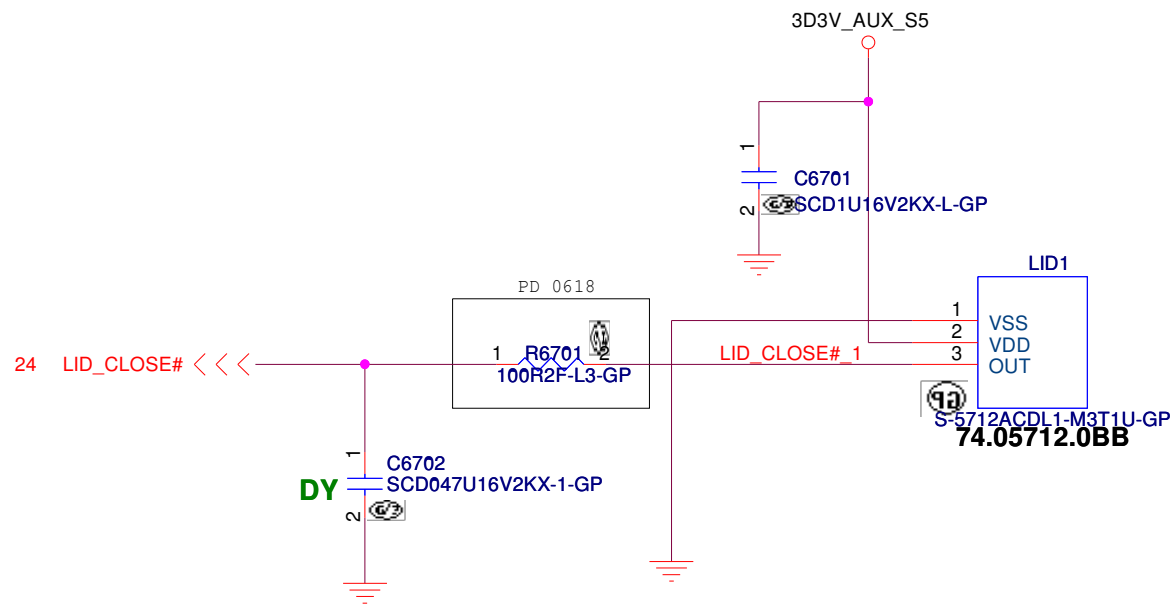
Rayleigh_SLS

Rev	S
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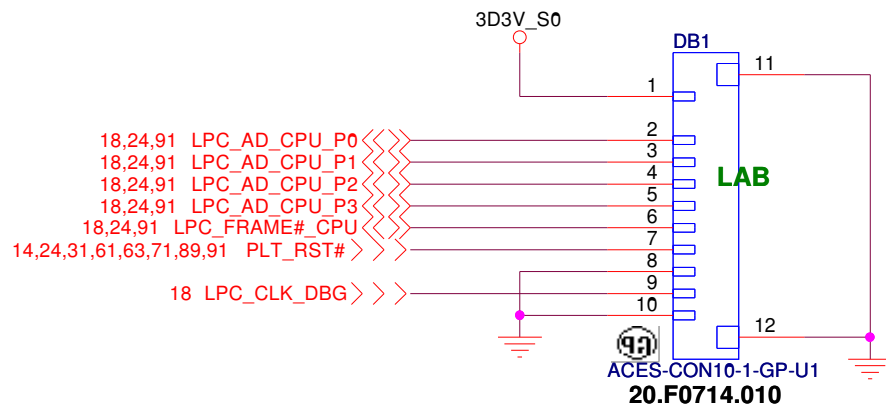


AFTP TESTPOINT


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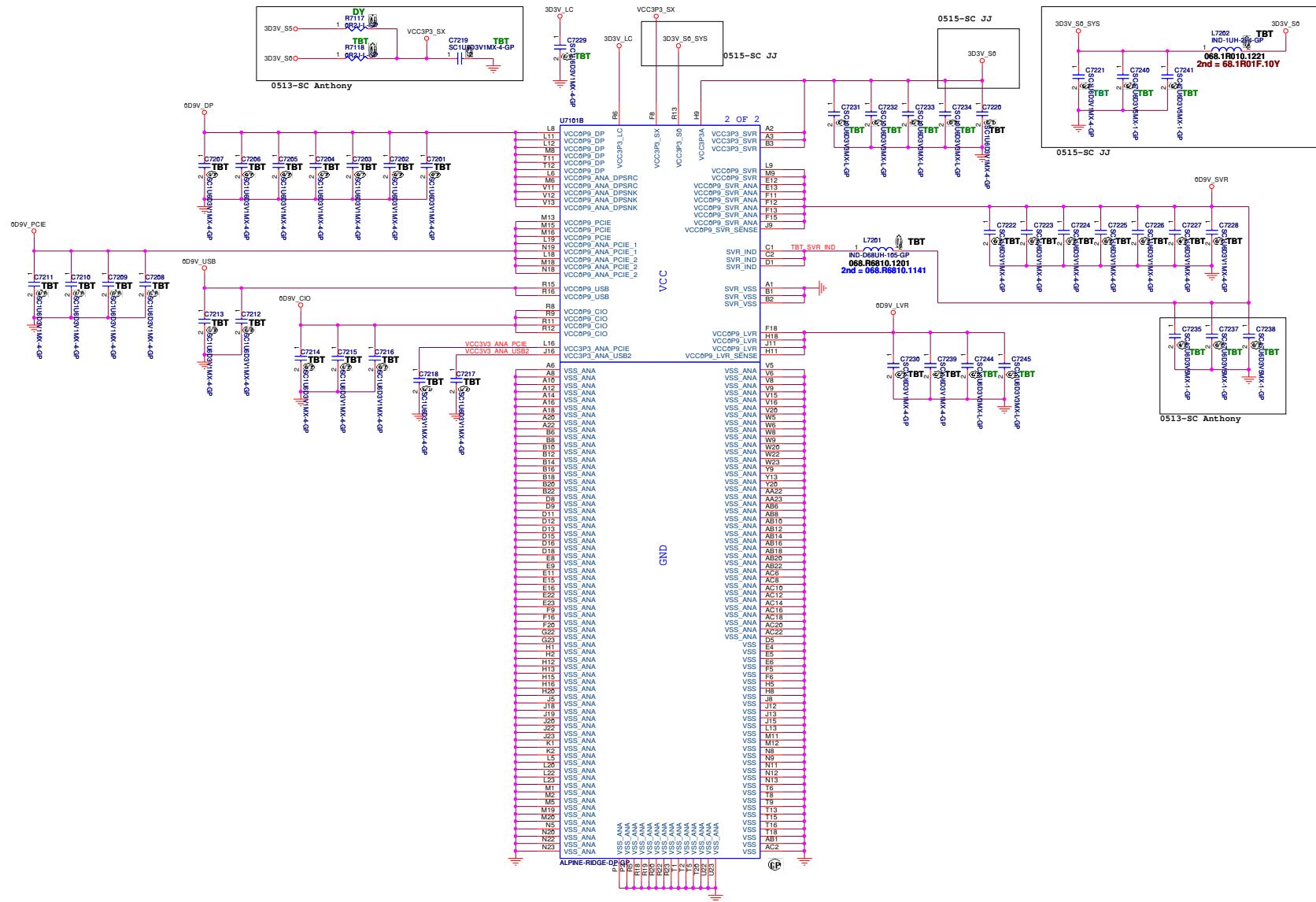
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<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Hall Sensor		
Size A	Document Number Rayleigh SLS	Rev SA
Date: Wednesday, August 12, 2015	Sheet 67 of	105



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Debug connector			
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Taipei Hsien 221, Taiwan, R.O.C.

File

Thunderbolt(2/5)

Size

Document Number

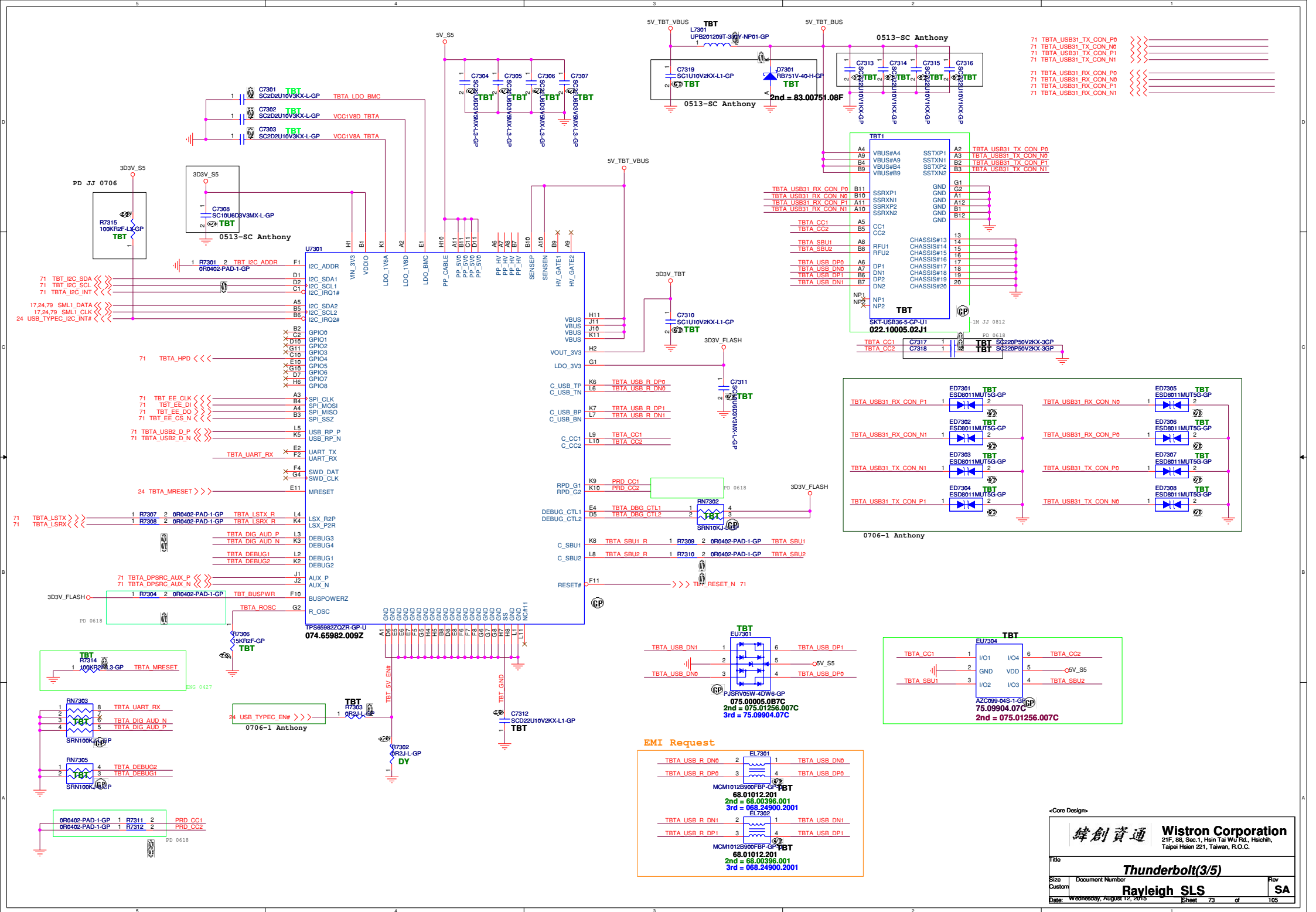
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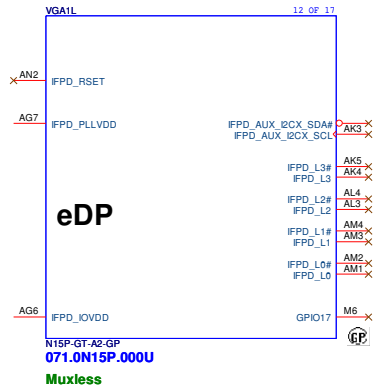
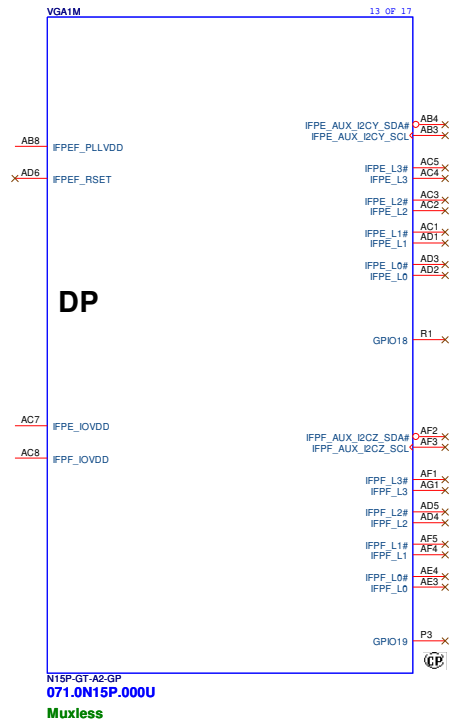
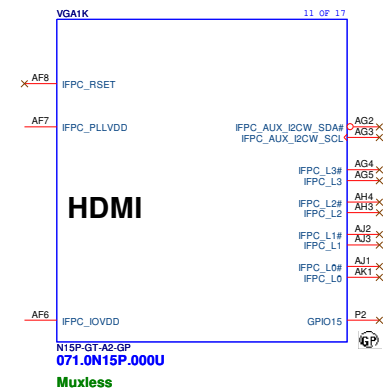
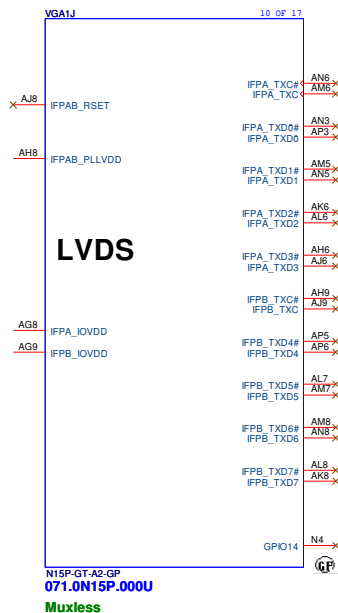
Rayleigh SLS

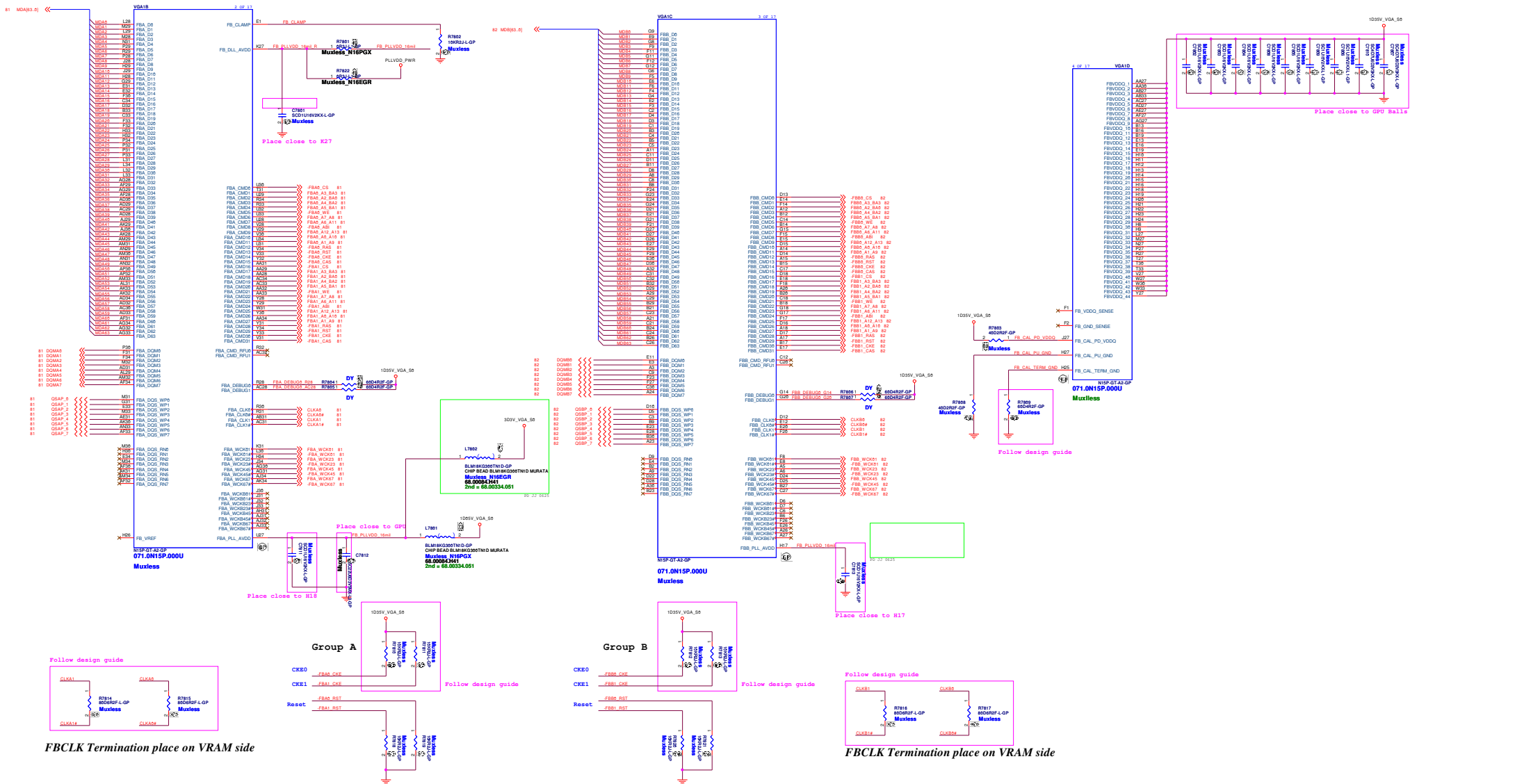
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Date: Monday, September 17, 2019

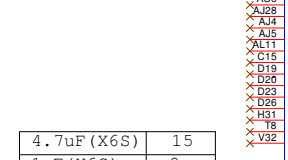
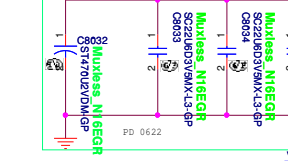
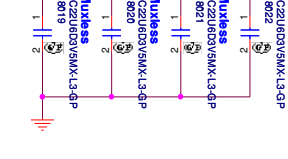
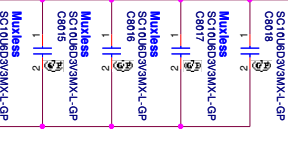
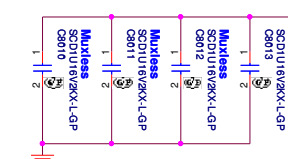
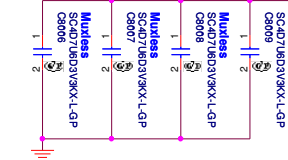
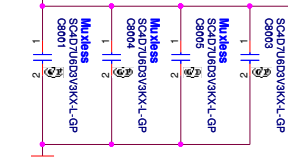
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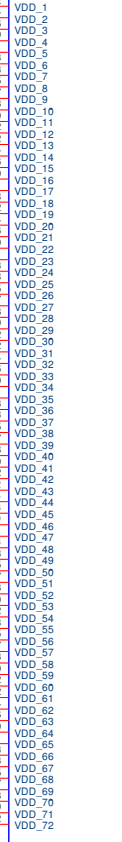


1V_VGACORE_S0



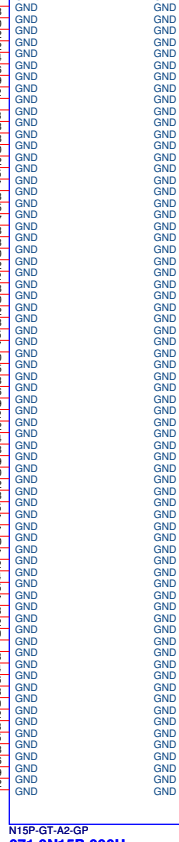
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VGA1E 5 OF 17



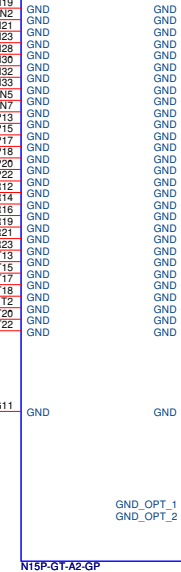
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Muxless

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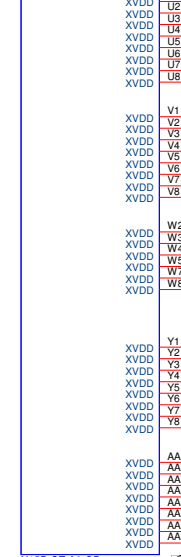
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VGA1I 9 OF 17



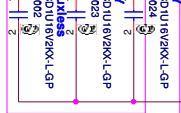
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VGA1H 8 OF 17

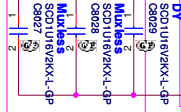


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Place near J8/K8



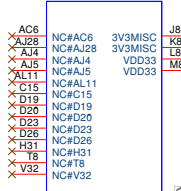
Place near L8/M8



Place near GPU



Place near GPU



N15P-GT-A2-GP
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Muxless

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Title

GPU_POWER/GND (5/5)

Size

Document Number

Rev

Custom

Rayleigh SLS

SA

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Wednesday, August 12, 2015

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of

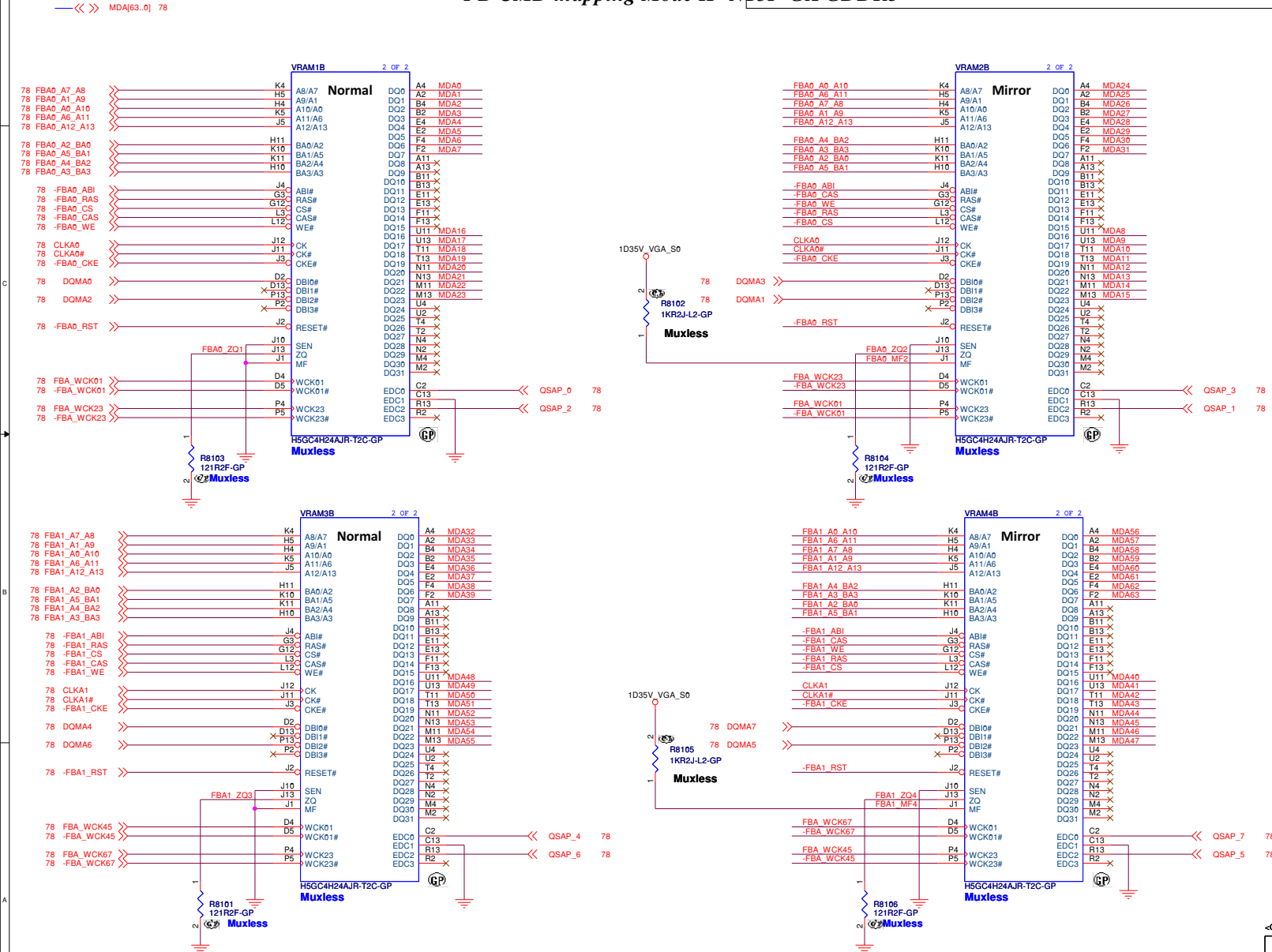
105

TABLE GDDR5 VIDEO MEMORY				
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	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

LOGIC

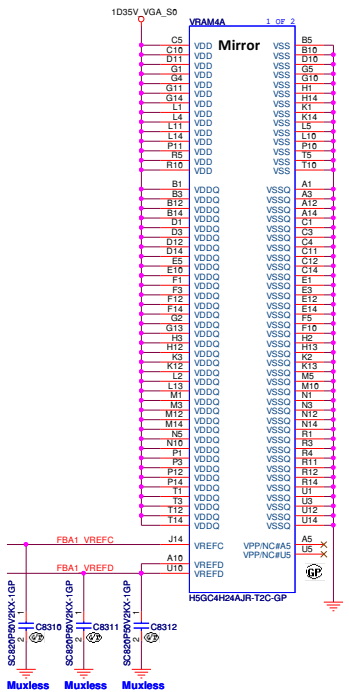
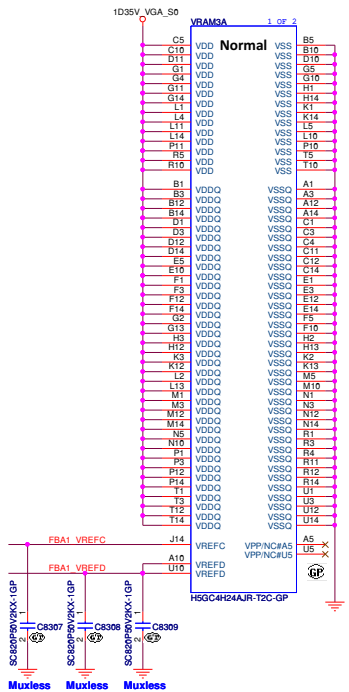
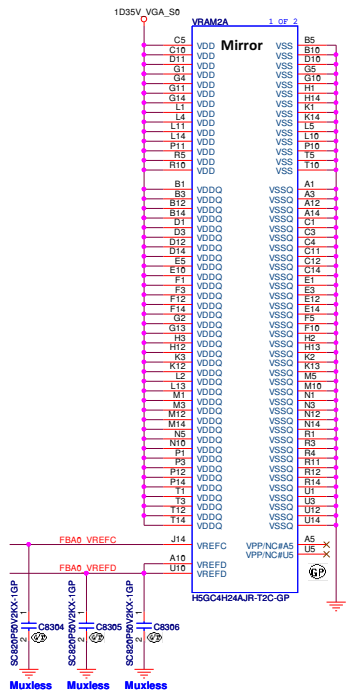
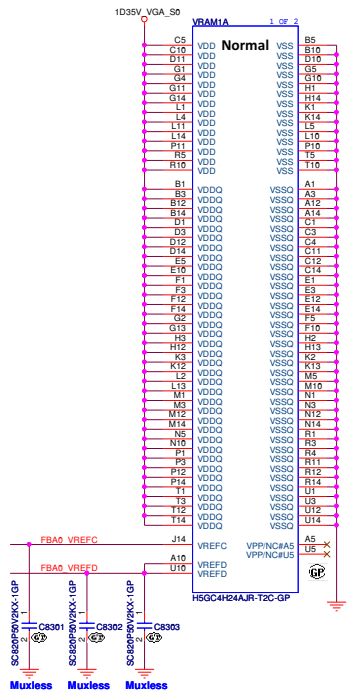
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FB CMD mapping Mode H -N15P-GX GDDR5

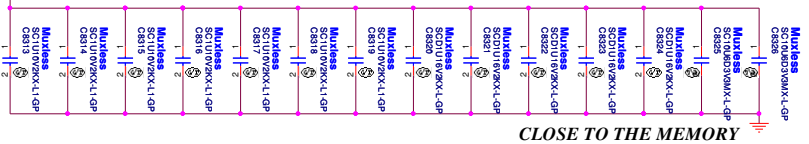


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Size	Document Number	Rayleigh_SLS	
Custom		Rev SA	
Date: Wednesday, August 12, 2015	Sheet 81	of 105	

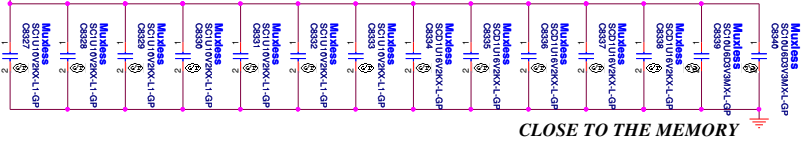


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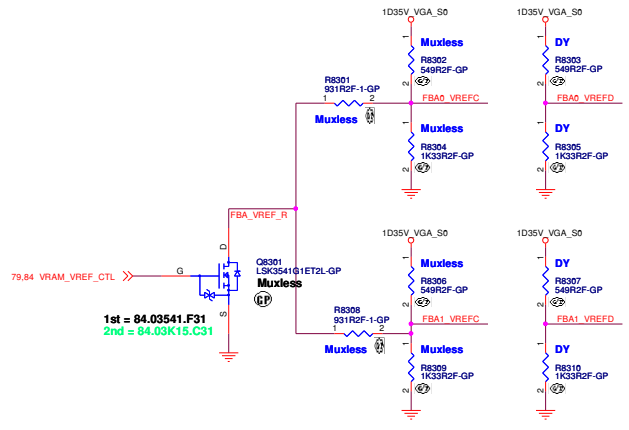


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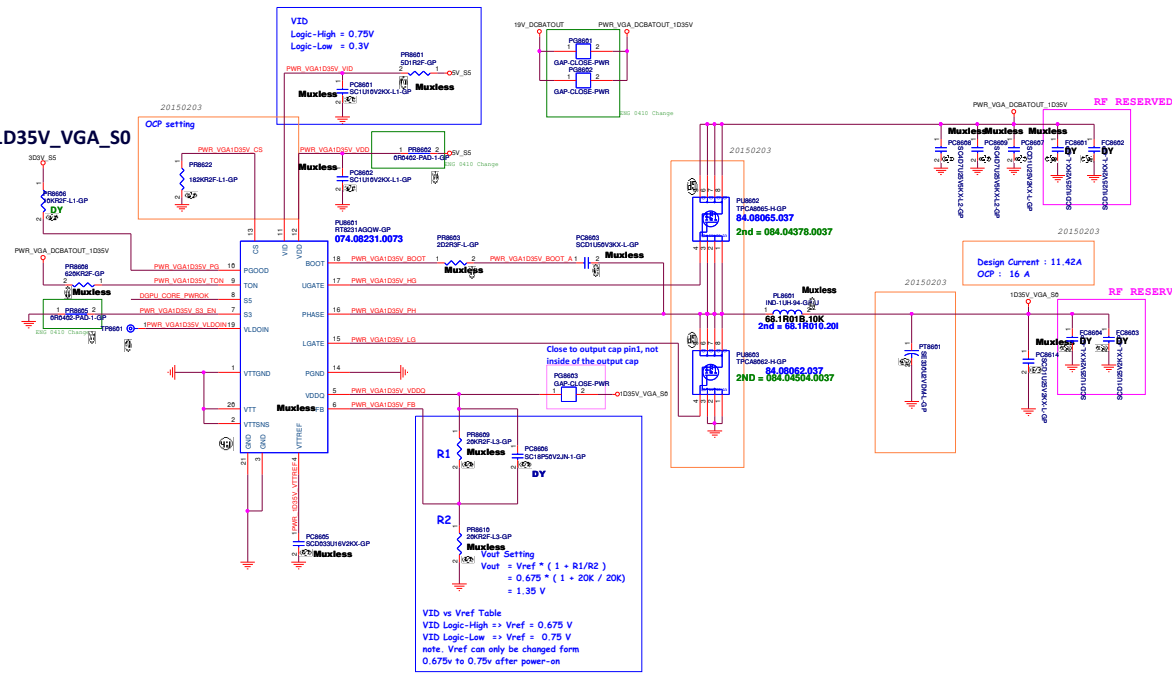
FOR VRAM3/ VRAM4



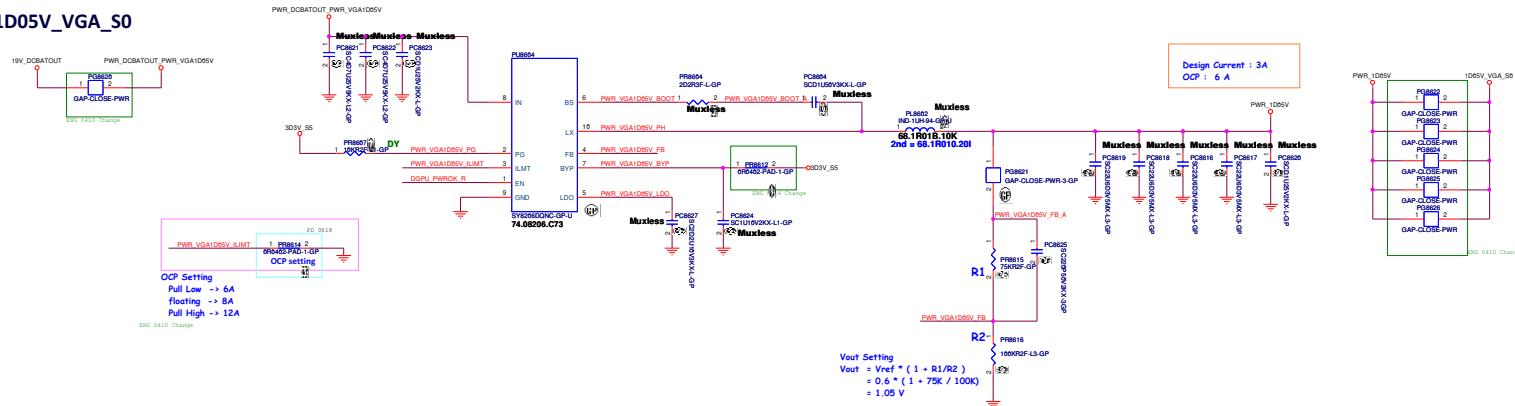
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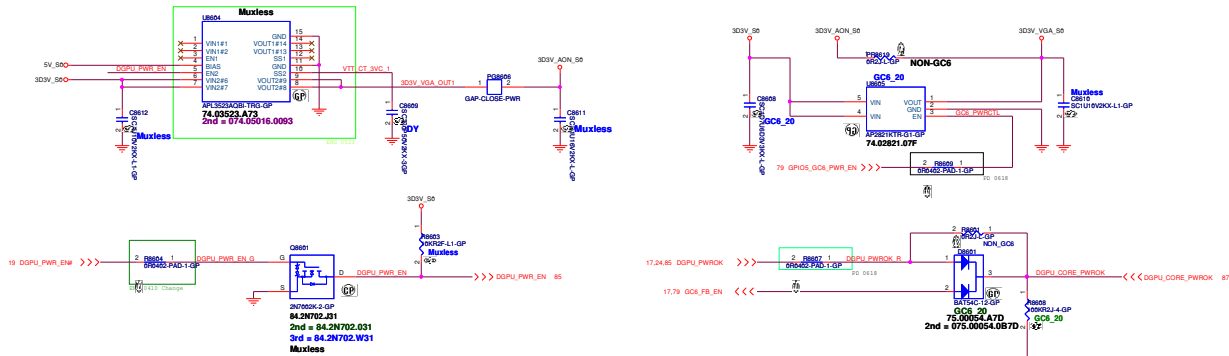
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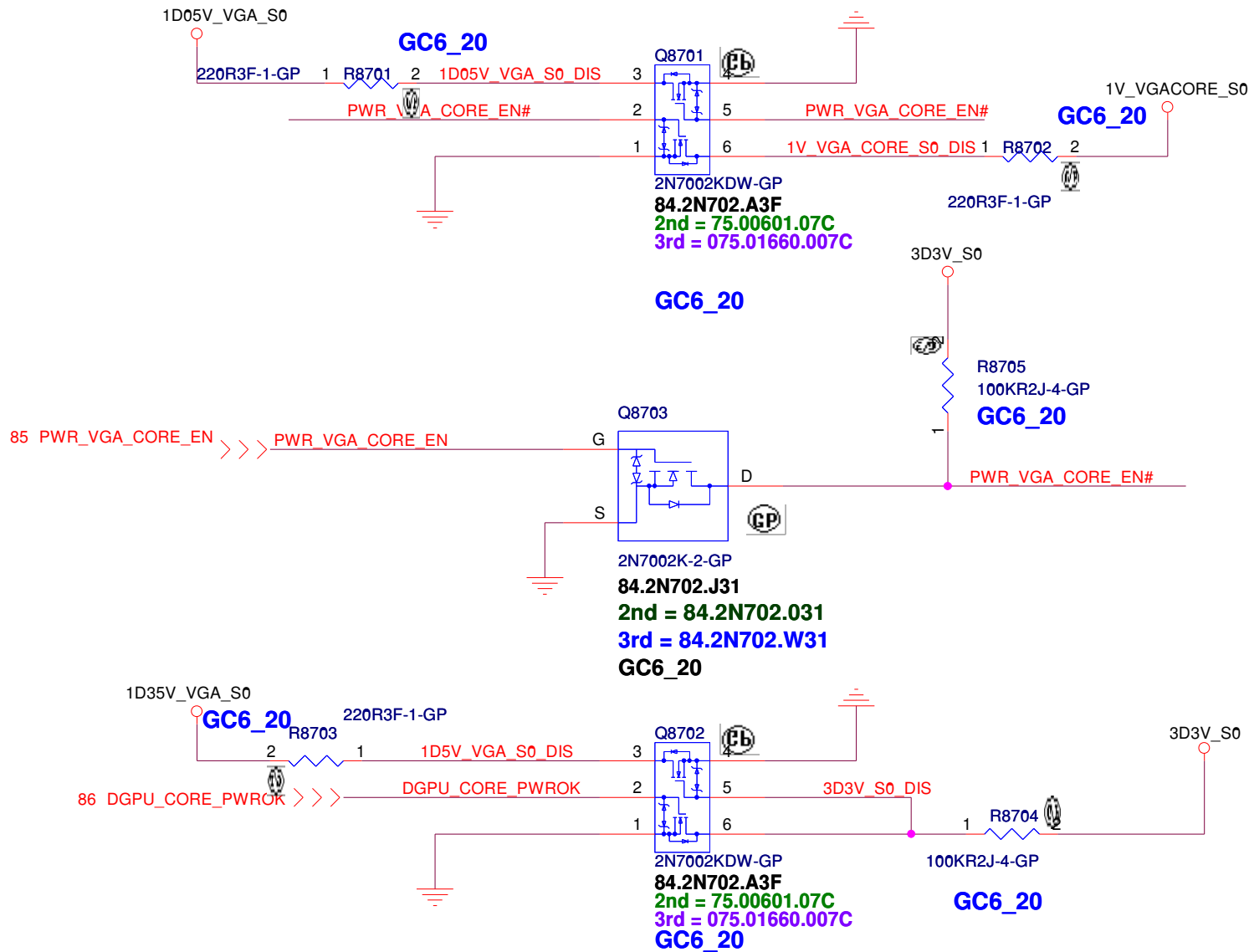


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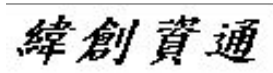


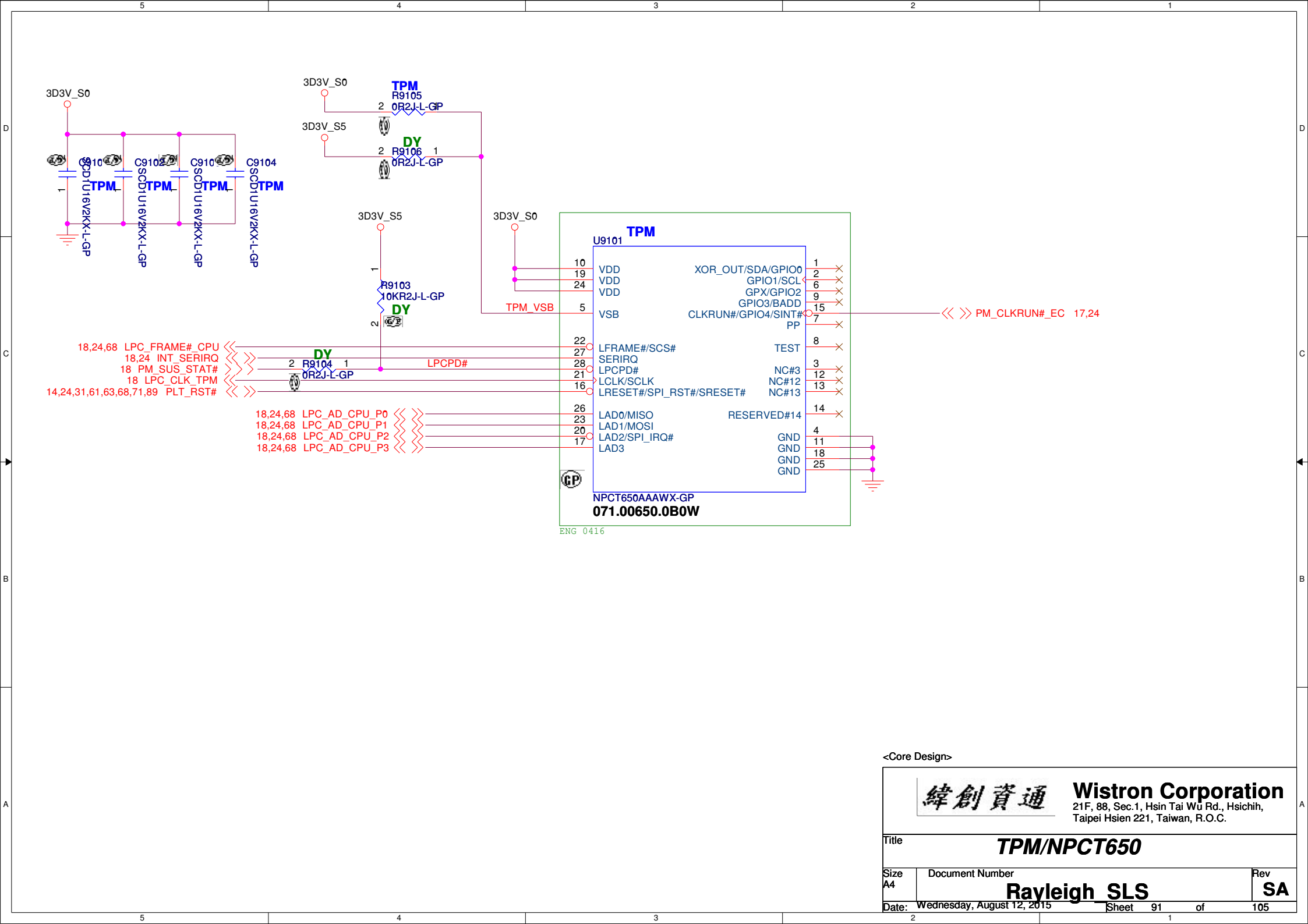
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Title			
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Size A	Document Number		Rev SA
Date: Monday, September 07, 2015		Sheet 87 of	105



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SizeA4	Document NumberRayleigh SLS
Date:Wednesday, August 12, 2015	RevSA
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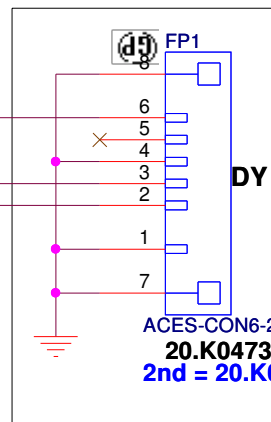
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15 USB_PCH_PP11
15 USB_PCH_PN11



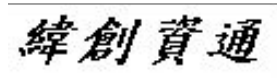
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ACES-CON6-21-GP
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0513-SC Anthony

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Title

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Size
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Document Number

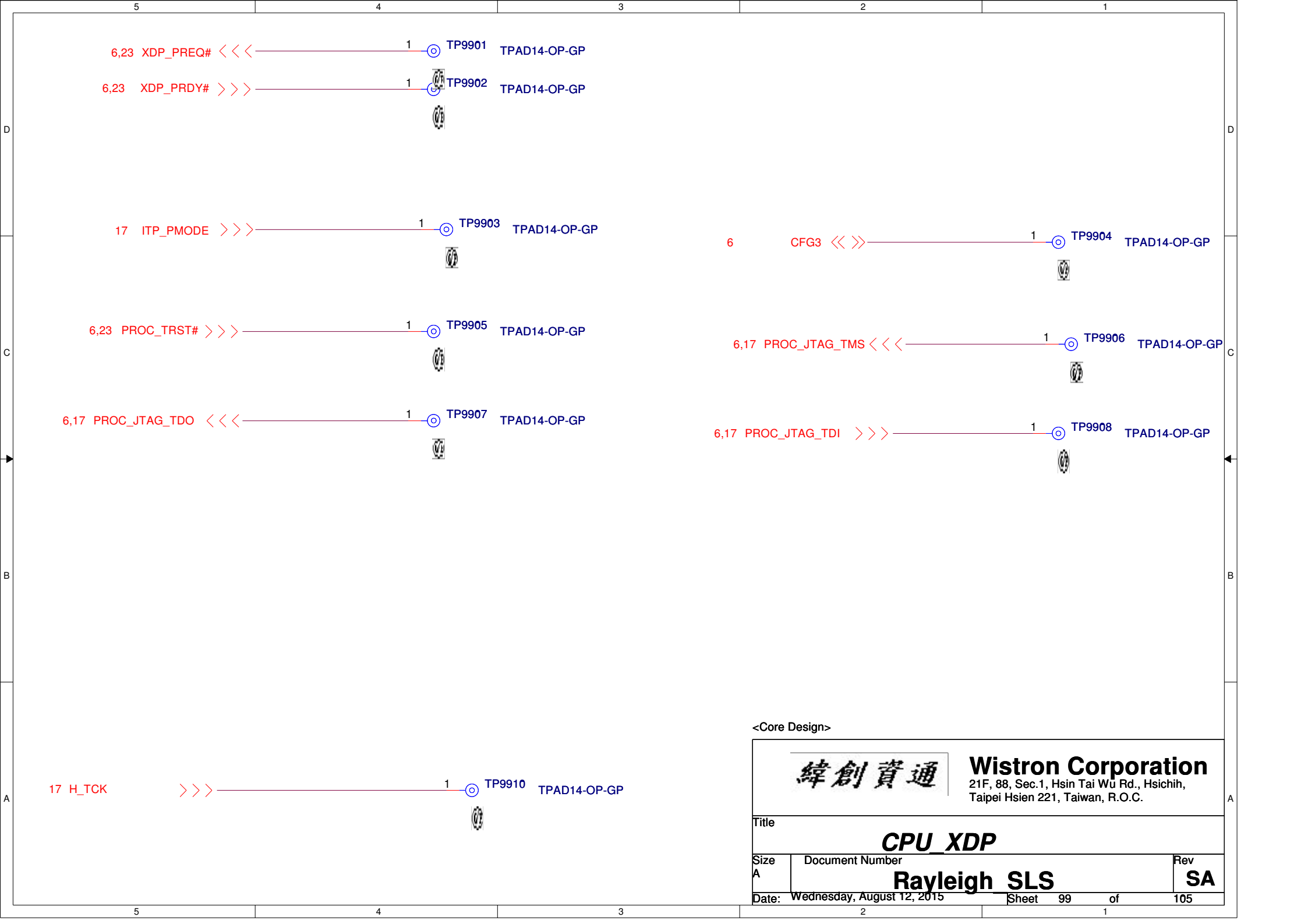
Rayleigh_SLS

Rev

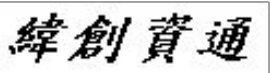
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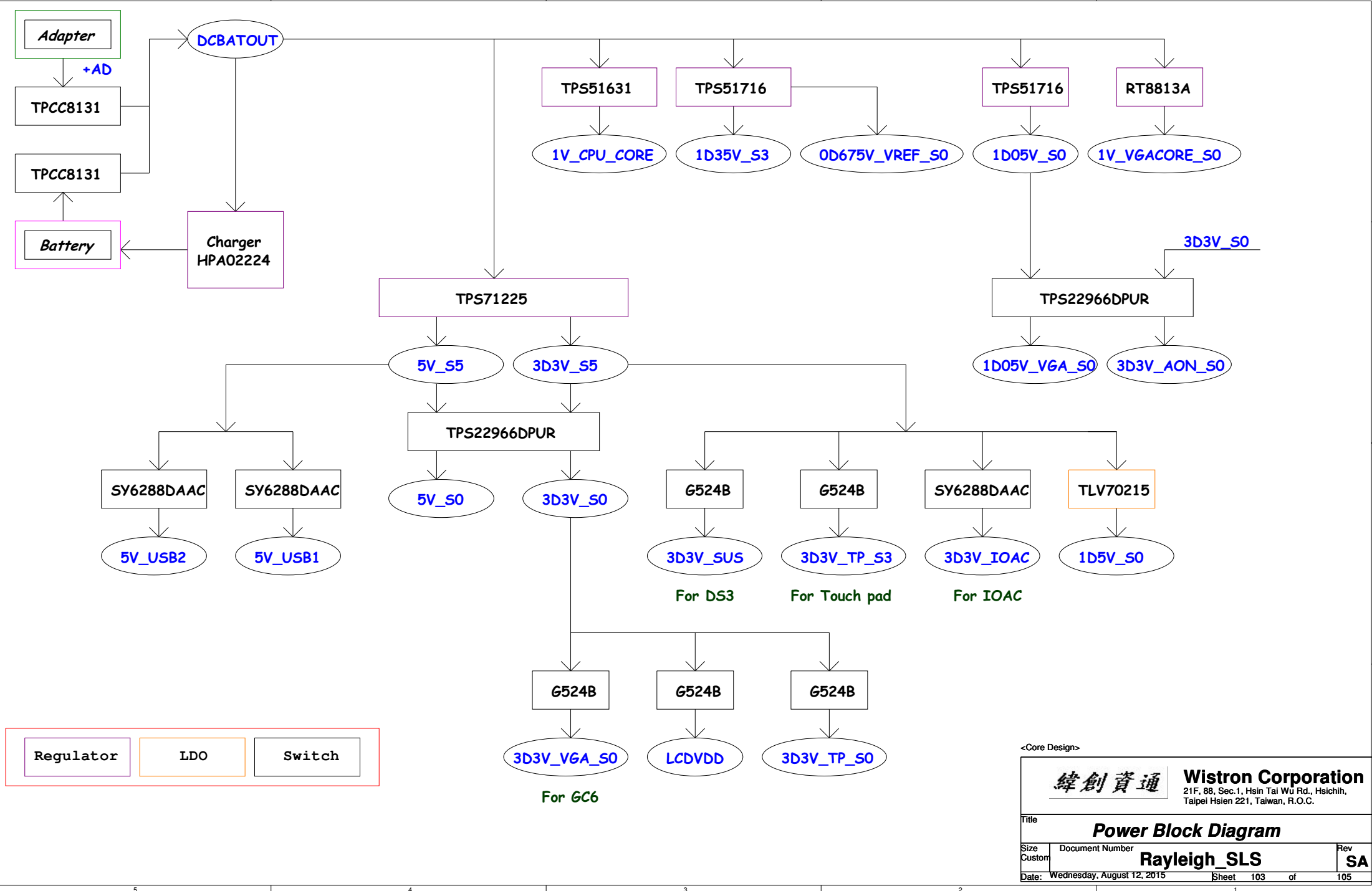
Date: Monday, September 07, 2015

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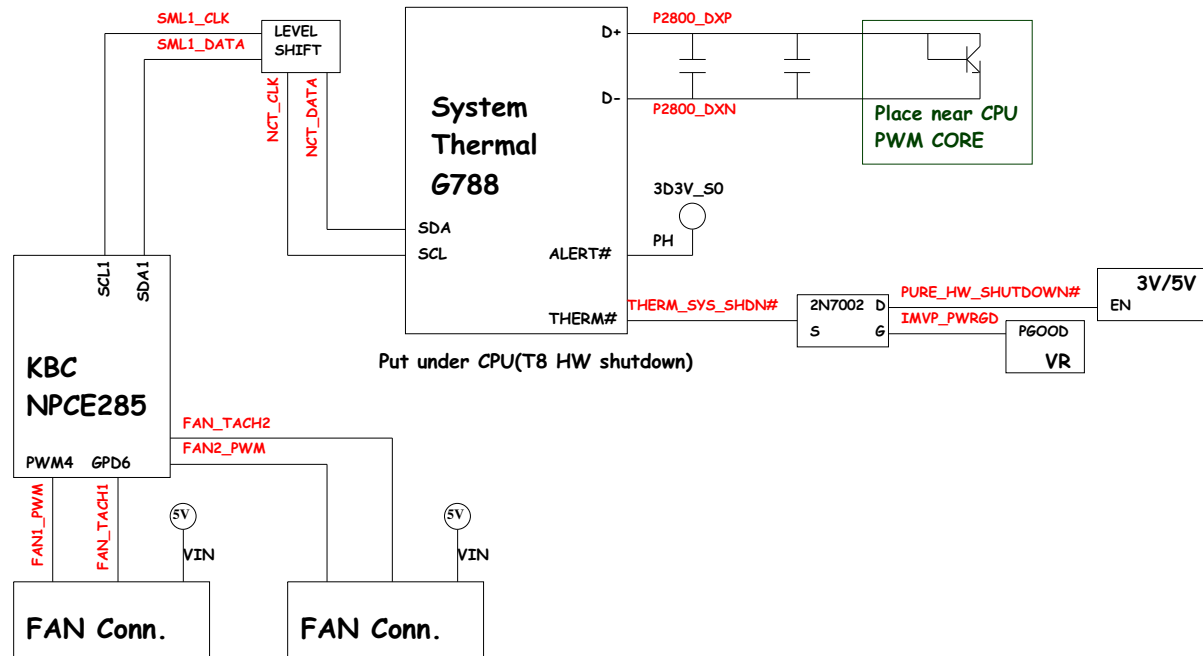


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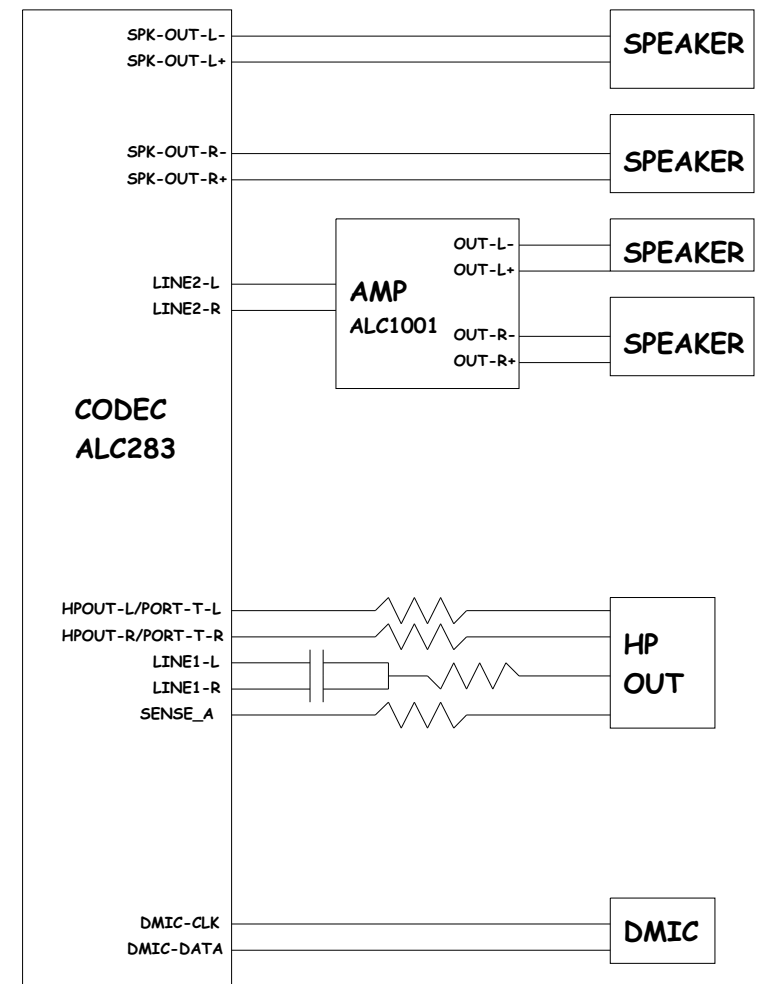
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Title CPU_XDP			
Size A	Document Number Rayleigh SLS		Rev SA
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Thermal Block Diagram



Audio Block Diagram



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Title Thermal /AUDIO Block Diagram			
Size Custom	Document Number EA40 HU ULT		Rev SA
Date: Wednesday, August 12, 2015	Sheet 105	of 105	